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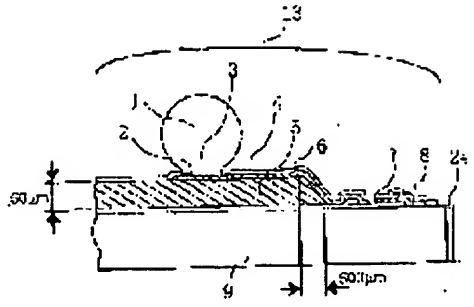
(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device for enabling flip chip connection without the need of an underfill.
SOLUTION: This semiconductor device is provided with a semiconductor element, an insulation layer formed by mask-printing an insulation material containing particles on the semiconductor element and an external connection terminal formed on the insulation layer and electrically connected to an electrode provided on the semiconductor element.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by having wiring which is formed the insulating layer which has the ramp formed by using a mask and printing an insulating material on the semiconductor device and this semiconductor device, the external connection terminal formed on this insulating layer, and on this insulating layer, and connects electrically the circuit electrode of this external connection terminal and this semiconductor device.
[Claim 2] The semiconductor device according to claim 1 characterized by said insulating layer having a particle

[Claim 3] The semiconductor device characterized by having wiring which is formed a semiconductor device, th insulating layer containing a particle which has the ramp formed on this semiconductor device, the external connection terminal formed on this insulating layer, and on this insulating layer, and connects electrically the circuit electrode of this external connection terminal and this semiconductor device.
[Claim 4] The semiconductor device according to claim 2 or 3 characterized by constituting said particle from same ingredient as the insulating material which forms said insulating layer.
[Claim 5] The path of said particle is a semiconductor device according to claim 2 or 3 characterized by being 1(micrometers or less.
[Claim 6] the semiconductor device according to claim 1 or 3 characterized by for the ramp and this insulating layer thickness of said insulating layer swelling in near the boundary of the flat part used as about 1 law, and having a part.
[Claim 7] The semiconductor device according to claim 1 or 3 characterized by said insulating layer thickness being about 35 micrometers thru/or about 150 micrometers.
[Claim 8] Said insulating layer thickness is a semiconductor device according to claim 1 or 3 characterized by being 1/20 to 1/5 of the thickness of said semiconductor device.
[Claim 9] The semiconductor device according to claim 1 or 3 with which the inclination of the ramp of said insulating layer is characterized by being about 5% thru/or about 30% to the circuit side of said semiconductor device.
[Claim 10] The elastic modulus of said insulating layer is a semiconductor device according to claim 1 or 3 characterized by being about 0.1 GPa(s) thru/or about 10 GPa(s).
[Claim 11] Said insulating layer is a semiconductor device according to claim 1 or 3 characterized by curing temperature consisting of about 100 Centigrade with the ingredient which is about 250 degrees.
[Claim 12] The semiconductor device according to claim 1 or 3 with which glass transition temperature of said insulating layer is characterized by being 400 degrees from 150-degree Centigrade.
[Claim 13] The semiconductor device according to claim 1 or 3 with which pyrolysis temperature of said insulating layer is characterized by being 450 degrees from 300-degree Centigrade.
[Claim 14] It is the semiconductor device which it has wiring which connects electrically the circuit electrode of an external connection terminal and this semiconductor device which was formed on the semiconductor device, the insulating layer formed on this semiconductor device, and this insulating layer, and was formed on this insulating layer, and the glass transition temperature of this insulating layer is 400 degrees from 150-degree Centigrade, and is characterized by the pyrolysis temperature of this insulating layer being 450 degrees from 300

degree Centigrade.
[Claim 15] Said insulating layer is a semiconductor device according to claim 1 or 3 characterized by consisting of polyimide, a polyamide, polyamidoimide, epoxy, a phenol, or silicone at least.
[Claim 16] The manufacture approach of the semiconductor device characterized by having the process which uses a mask, prints an insulating layer and forms it on a wafer.
[Claim 17] The manufacture approach of the semiconductor device characterized by to have the third process which forms the external connection terminal electrically connected with the first process which uses a mask, prints an insulating layer and forms it on a wafer, the second process which forms wiring ranging over the ramp and flat part of this insulating layer from the circuit electrode of this wafer, this wiring, and a circuit electrode on this insulating layer.
[Claim 18] The manufacture approach of the semiconductor device characterized by to have the first process which uses a mask, prints an insulating layer and forms it on a wafer, the second process which form a pad on this insulating layer, the third process which form wiring which connects electrically the circuit electrode and thi pad of this wafer on this insulating layer, and the fourth process which form an external connection terminal on this pad.
[Claim 19] The manufacture approach of a semiconductor device given in either of claims 16-18 characterized b said insulating layer having a particle.
[Claim 20] The manufacture approach of a semiconductor device given in either of claims 16-18 characterized b forming an insulating layer by printing two or more times using said mask.
[Claim 21] The manufacture approach of a semiconductor device given in either of claims 16-18 characterized b moving a squeegee to the top-most vertices which counter from top-most vertices to opening of said mask in saic first process, and printing and forming said insulating layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the structure and the manufacture approach of a semiconductor device aiming at flip chip bonding.
[0002]
[Description of the Prior Art] Many of semiconductor devices have a laminated structure, and the insulating laye is arranged between each class in many cases. Opening is prepared in this insulating layer, it lets that opening pass, and wiring which connects a lower layer terminal and the upper terminal is formed.
[0003] The following approaches are adopted as the insulating stratification approach. That is, a photosensitive insulating material is applied with a spin coat method on a semiconductor device, and opening of an insulating layer is formed by carrying out exposure and development. Moreover, metal wiring which connects a lower laye terminal and the upper terminal applies the second photosensitive ingredient to the insulating-layer upper layer, forms a mask by performing exposure and development to this, and forms metal wiring which connects the terminal and the upper layer of the insulating-layer lower layer in using together processes, such as this, plating, spatter, CVD, and vacuum evaporationo. This is removed after becoming unnecessary [the photosensitive insulating material used as a mask].
[0004] Formation of wiring which connects the terminal in the lower layer of an insulating layer and the upper layer according to the above process is attained. The fragmentary sectional view of the semiconductor device formed of such a process is shown in drawing 31 . In this drawing, the aluminum pad 7 serves as a terminal of insulating-layer 12 lower layer, and the bump pad 3 serves as a terminal of the insulating-layer upper layer. And as for the insulating layer 12 formed on the wafer 9 with which the semi-conductor was formed, opening is prepared on the aluminum pad 7. Moreover, the metal wiring 11 is formed from the aluminum pad 7 even to the bump pad 3 of the upper layer of an insulating layer 12. The bump 10 is formed in the bump pad 3. In addition, i is called rewiring to form wiring from the aluminum pad 7 to the bump pad 3 in this way. Moreover, the thickness of the insulating layer 12 in this case is almost equivalent to the thickness of the metal wiring 11.
[0005] Flip chip bonding is in one of the gestalten which mount the semiconductor device manufactured through such a process on the circuit board like a printed wired board, and are connected. Drawing 32 is the sectional view of the semiconductor device which carried out flip chip bonding. Connection between a semiconductor device 13 and the circuit board 14 is made because the bump 10 prepared on the terminal of a semiconductor device 13 solidifies again after melting on the circuit board. The gap of a semiconductor device 13 and the circui board 14 is filled up with the resin of high rigidity. In addition, this resin is called under-filling 15 and is effectiv in reinforcing a connection. There is JP,11-111768,A as an example of the flip chip bonding which carried out under-filling.
[0006]
[Problem(s) to be Solved by the Invention] However, there are the following problems in the above-mentioned conventional technique.
[0007] Difficulty is in the supply approach of the resin to the gap of a semiconductor device and the circuit boar in the first place. That is, the method of using capillarity is taken as an approach a clearance supplies resin to the gap which is generally 0.3mm or less. However, since the resin ingredient for under-filling is hyperviscous

liquefied resin, it requires the time amount embedded in a clearance, and has the problem of an air ball tending to remain.
[0008] Difficulty is [second] in removal of a semiconductor device. That is, in order that the hardened under-filling ingredient may remain on the circuit board even after removing even if it removes this semiconductor device from on the circuit board when the semiconductor device linked to the circuit board is a defective, the problem that playback of the circuit board is difficult exists.
[0009] Also in order to solve the first and the second trouble, it is desirable to connect a semiconductor device to the circuit board, without carrying out under-filling. However, under-filling is carried out in order to prevent destruction of the connection resulting from distortion produced in the connection by generation of heat at the time of using the completed electric product etc., and in not carrying out, the problem that the connection life of semiconductor device will become extremely short arises. Moreover, when forming a solder bump in the semiconductor device which makes possible unnecessary flip chip bonding of under-filling, by collapse of the impurity contained in the solder bump, alpha rays occur and malfunction of the transistor section may be caused.
[0010] The purpose of this invention is to realize the semiconductor device which makes possible unnecessary flip chip bonding of under-filling.
[0011]
[Means for Solving the Problem] This invention is constituted as a claim, in order to attain the above-mentioned purpose. Thus, the above-mentioned purpose is attained by forming wiring on a desired insulating layer (thick-film insulating layer). For example, destruction of a connection can be prevented by using the ingredient of low elasticity for the insulating layer of a semiconductor device, and forming an insulating layer with a thickness of 35 microns or more. Moreover, it becomes possible to reduce sharply the stress produced in a connection in the insulating layer of low elasticity existing. By this, the connection life of a semiconductor device improves sharply. Moreover, not only easing the stress produced to a wafer etc. but unnecessary alpha rays can be intercepted by making an insulating layer into predetermined thickness. [0012] Moreover, when adopting the insulating layer of the thick film of about 35 micrometers or more, it is hard to apply the conventional wiring formation approach. Since the ingredient for insulating stratification is hyperviscosity, it will become an insulating layer containing air bubbles, and will stop that is, achieving the function as an insulating layer in a spin coat method, when carrying out thick-film formation of the insulating layer. Even if it develops the new thick-film formation approach apart from this, since the permeability of light falls, in 35-micrometer thickness, it is difficult to carry out pattern formation of the opening of an insulating layer etc. with high precision in exposure development. ****** this problem is solvable -- the side attachment wall of opening of an insulating layer -- ** beyond about 80 degrees and it -- since that height serves as a sharply larger value than wiring thickness perpendicularly, metal wiring becomes that it is hard to be formed in a side attachment wall. Moreover, since the flection of metal wiring is formed in the boundary section of a side attachment wall and the upper layer even when it is able to form even if, it is easy to concentrate stress on this location, and, for this reason, a crack tends to progress. For this reason, the connection life at the time of circuit board connection will become short.
[0013] Since the flection of metal wiring which a thick-film insulating layer is formed, and formation of wiring on an insulating layer is attained with the conventional method of construction by making the configuration of insulating-layer opening into a gently-sloping slant face, and stress concentrates there by carrying out mask printing of the insulating material containing a minute particle does not exist, either, it is hard to produce an open circuit of wiring. Moreover, the property of a thick-film insulating layer is changed in the thickness direction. For example, near is carried out to the property of a substrate of carrying the property of a thick-film insulating layer by the semiconductor device side, and carrying these in a semiconductor device by the near and electrode side. As stress does not concentrate on wiring formed on the thick-film insulating layer by this, dependability can be raised further. That is, an open circuit can be controlled further. In addition, on these specifications, this thick-film insulating layer is indicated to be a stress relaxation layer.
[0014]
[Embodiment of the Invention] Hereafter, it explains, using drawing together about one example of this invention. In addition, in all drawings, in order that the same sign may have omitted the explanation which overlaps since the same part is shown and may give explanation easy, it has changed the proportion of each part with the actual condition.

[0015] First, the structure of the semiconductor device by this example is explained. Below, although it is collectively manufactured by many per wafer, in order to give explanation easy, a semiconductor device takes ou the part and is explained. The fragmentary sectional view of the semiconductor device 13 of this example is shown in drawing 1 .

[0016] The wafer 9 with which the semiconductor circuit was formed is a wafer which ended the last process as used in the field of a semi-conductor production process, and is a thing before division cutting at many semiconductor devices 13. The connection terminal 7 for the exteriors, for example, an aluminum pad, is formed in each semiconductor device 13. In the semiconductor device 13 of a conventional type, when storing in semiconductor packages, such as QFP (Quad Flat Package), this aluminum pad 7 connects a golden wire etc., and it is used in order to realize a flow with the external terminal of a semiconductor package. The front face of a semiconductor device 13 in which the semiconductor circuit was formed is covered with the protective coat 8 except for the cutting section 24 at the time of cutting the wafer 9 with which the aluminum pad 7 top and many semi-conductors were formed to the chip-like semiconductor device 13, and its circumference. The insulating resin which becomes this protective coat 8 from the insulating resin independent or the organic material which consists of thickness 1 thru/or an about 10-micrometer inorganic material is used together. The bipolar membran which carried out the laminating of the organic compound insulator which becomes the upper part of independence or said inorganic insulator layer from an organic material about the insulator layer which consists of thickness 1 thru/or an about 10-micrometer inorganic material is used for this protective coat 8. When using this bipolar membrane, as for this organic film, it is desirable to use a photopolymer ingredient. When a photosensitive ingredient suitable as organic film of a protective coat 8 is illustrated by this example, there are photosensitive polyimide, photosensitive benz-cyclo-butene, photosensitive poly benzoxazole, etc. In this example, the inorganic material, the organic materials, or such bipolar membrane of well-known common use can be used not only as this but as a protective coat. For example, SiN, SiO2, etc. can be used as inorganic film. Moreover, although it does not matter even if it is formed so that the whole surface may be covered mostly, of course, as shown in drawing 33 , even if this organic film is formed only in the field of the inorganic film which becomes near the aluminum pad 7, it is not cared about, and as shown in drawing 34 , it may be formed only in two or more places of the arbitration of an inorganic film front face. Thus, by limiting the field of the organic film, the curvature of the wafer 9 by the internal stress of a protective coat 8 is reduced, and it becomes advantageous in respect of the handling in a production process, focusing at the time of exposure, etc. In addition in this example, the field near the aluminum pad 7 has pointed out the field from the edge of the aluminum pad 7 to 1mm of maximum distances. In addition, in drawing 33 and drawing 34 , although the organic film around the aluminum pad 7 is formed in the continuation field, it may be formed in the field which became independent for each aluminum pad of every, respectively. Specifically, it becomes a field like drawing 35 . In view of the patter precision of the photopolymer used for this organic film, membranous internal stress, and the component property of this semiconductor device, it determines whether which gestalt of drawing 35 is used from drawing 33 . If an example of the component property said here is given, it has pointed out changing the level of the energy barrier in each active cell inside a component (transistor) according to the stress operation to this semiconductor device.

[0017] On the protective coat 8, thickness 35 thru/or the 150-micrometer stress relaxation layer 5 are formed alternatively. Although the thickness of a stress relaxation layer is dependent on the size of a semiconductor device, the elastic modulus of a stress relaxation layer, semiconductor device thickness, etc. and cannot generally be ******(ed) The semiconductor device thickness generally used is about 150 thru/or 750 micrometers. The place which conducted the stress simulation experiment with the bimetal model which consists of a semiconductor device and a stress relaxation layer formed in the front face, Since, as for necessary stress relaxation layer membrane thickness, it turned out that 10 thru/or 200 micrometers are 35 thru/or 150 micrometers desirable still more preferably, this example was formed in this thickness range. About 1/of this is equivalent to about 20 to 1/5 thickness to the thickness of a semiconductor device. If thickness becomes smaller than 35 micrometers, desired stress relaxation cannot be obtained, and if thickness becomes thick exceeding 150 micrometers, the curvature of a wafer will occur for the internal stress which stress relaxation layer 5 self has, and it becomes easy to generate the handling fault in focus gap, a wiring formation process, etc. in an exposure process etc., and there is a problem that productivity falls. The stress relaxation layer 5 is formed with the resin

ingredient which has the elastic modulus of 0.1GPa(s) to 10GPa(s) in an elastic modulus sharply smaller than a semiconductor wafer 9, for example, a room temperature. If it is the stress relaxation layer which has the elastic modulus of this range, a reliable semiconductor device can be offered. That is, in the case of the stress relaxation layer of the elastic modulus which is less than 0.1GPa, in case it becomes difficult to support the weight of the semiconductor device itself and it uses it as a semiconductor device, it is easy to produce the problem that a property is not stabilized. On the other hand, when the stress relaxation layer of the elastic modulus exceeding 10GPa is used, there is even a danger that the curvature of a wafer will occur for the internal stress which stress relaxation layer 5 self has, will become easy to generate the handling fault in focus gap, a wiring formation process, etc. in an exposure process etc., and the fault that a wafer breaks further will occur. The edge section of the stress relaxation layer 5 has the inclination, and the average gradient is 5 thru/or about 30%. In the case of the tilt angle which is less than 5%, an inclination becomes long too much and desired thickness is not obtained. For example, in order to consider as the thickness of 100 micrometers with the tilt angle of 3% of average gradients, desired thickness will be obtained, if about 7 millimeters cannot be found when the horizontal distance of 3-millimeter ** is needed and the edge section on either side is united. On the other hand, although it is satisfactory in respect of horizontal distance when a tilt angle is 30% **, the danger that step coverage conversely sufficient in the case of wiring formation will not be obtained is high. Especially plating resist is attached, there is no process margin in the process of the surroundings, exposure, and development, and special skill or a special technique is needed. When a tilt angle is still larger, the so-called stress concentration effectiveness may act, stress may concentrate on the edge section, the inclination an open circuit of the wiring 4 for rewiring becomes easy to generate in the edge section as the result may appear, and a device special to wiring structure may be needed. Since it is 50-micrometer thickness from the edge of the stress relaxation layer 5 with the horizontal distance of 500 micrometers in the case of drawing 1 , an average gradient is 10%. The wiring 4 for rewiring is formed with conductors, such as copper, and has connected the aluminum pad 7 and the letter electrode 3 of a projection of stress relaxation layer 5 front face, for example, a bump pad. Moreover, the bump pad 3 top may form the gilding 2 for preventing oxidation of the bump pad 3. The front face of a semiconductor device 13 is covered by the surface protective coat 6 except for the cutting section 24 at the time of cutting the wafer 9 with which the bump pad 3 and many semi-conductors were formed to each semiconductor device 13.

[0018] Since it is closing by covering completely a protective coat 8 and the stress relaxation layer 5 by the surface protective coat 6, it prevents that a protective coat 8 and the stress relaxation layer 5 exfoliate from the front face of a wafer 9 in which the semiconductor device was formed, and invasion of foreign matters, such as ion which causes the performance degradation of a semi-conductor, can also be mitigated. Moreover, since the protective coat 8, the stress relaxation layer 5, and the surface protective coat 6 are all retreating from the cutting section 24, in case they carry out cutting separation of the semiconductor device 13, they do not receive damage.

[0019] The various resin ingredients which have an electrical insulating characteristic as a surface protective coat 6 can be used. Although it is desirable that it is a photosensitive ingredient since it is necessary to form a pattern, membranes may be formed by printing, for example using the ingredient corresponding to high precision printing of an ink jet etc. In addition, after carrying out solid formation of the insulator layer by the cheap methods of application, such as a curtain coat, a photolithography process may be used, and patterning of the etching resist may be formed and carried out, and membranes may be formed through the process of etching processing and resist exfoliation for the above-mentioned insulator layer using this resist pattern. Although various ingredients are usable in this example as such an ingredient, if some are illustrated, denaturation triazole resin, denaturation melamine resin, polyimide resin, etc. will be suitably used as (1) photosensitivity ingredient as polyamidoimide resin, polyimide resin, and a charge of (3) solid membrane formation material as an acrylic denaturation photosensitivity epoxy resin, photosensitive polyimide resin, and a (2) ink-jet printing ingredient. If it illustrates still more concretely about a photosensitive ingredient, the photosensitive polyimide used for surface covering of a solder resist or a flexible printed circuit board used suitably will be suitably used as a surface protective coat 6 by the printed circuit board production process as a cheap photopolymer ingredient. On the other hand, as a charge of solid membrane formation material, photograph NISU TM of Toray Industries, Inc. etc. is suitable, for example. In addition, the solder resist was used in this example. The bump 1 is formed on the bump pad 3. As for this bump 1, forming with a solder ingredient is common. A bump 1 becomes an external connection terminal here.

[0020] The top view which omitted the bump 1 who originally exists the condition that the semiconductor device 13 shown in drawing 2 by drawing 1 is continuously formed on the wafer showed. The part shown by hatching in drawing 2 is the solder resist which is the surface protective coat 6. Moreover, it is formed in the condition that the stress relaxation layer 5 is formed in the shape of [which rounded off the angle] a rectangle, and gets down, and the cutting section 24 which is cutting at the time of separating each semiconductor device 13 exists between each semiconductor device 13. cut -- it is desirable to be located in 10 thru/or 100 micrometers from the edge of ** 6, for example, a surface protective coat. If there is an inclination which becomes easy to induce a chipping and it becomes conversely longer than 100 micrometers in case each semiconductor device will be separated, if shorter than 10 micrometers, an effective area usable as a semiconductor device will decrease. Therefore, it is desirable to locate spacing with the surface protective layer 6 in 10 thru/or 100 micrometers by this example as cut and carry out for the improvement in the yield of a semiconductor device 13. In addition, although not illustrated by the lower layer of the end of the wiring 4 for rewiring, the aluminum pad 7 exists in it.
[0021] According to this semiconductor device structure, since the stress relaxation layer 5 exists between the wiring 4 for rewiring, and a wafer 9, a semiconductor device 13 is connected on the circuit board 14, and in case it operates, it becomes possible to distribute distortion by the heat which a bump 1 receives. For this reason, it becomes possible to prolong a connection life, without carrying out under-filling 15, even if it carries this semiconductor device 13 in the circuit board 14. Moreover, since the stress relaxation layer 5 has the gently-sloping ramp, the wiring flection which turns into stress raisers in the middle of the wiring 4 for rewiring does not exist.
[0022] An example of the production process of the semiconductor device 13 in this example is explained using drawing. By drawing 3 , drawing 4 explains the sixth process from the fourth process, and drawing 5 explains the ninth process for from the first process to the third process from the seventh process. In addition, also in which drawing, cross-section structure of the semiconductor device 13 in this example is used as the sectional view which took out the part so that intelligibly.
[0023] The first process: Manufacture at the same process as the conventional semiconductor device 13 about the wafer 9 with which the semi-conductor whose aluminum pad 7 for external connection is formation ending was formed. Although the quality of the material of the pad for external connection was aluminum in the semiconductor device used by this example, an external connection pad may be copper. It is because wirebondin is not used as external connection, so it is not necessary to take into consideration the problem of the bonding nature which is easy to produce when an external connection pad is copper in this example. Since the electric resistance of wiring can be reduced if an external connection pad is copper, it is desirable also from a viewpoint of the improvement in an electrical property of a semiconductor device.
[0024] The second process: Form a protective coat 8 if needed. A protective coat 8 may already be formed in the so-called last process in a semi-conductor production process using an inorganic material, and also on an inorganic material, an organic material may be used for it and it may form it in plies. In this example, on the silicon dioxide formed of the silicon nitride formed by the insulator layer which consists of an inorganic material formed at the so-called last process in a semi-conductor process, for example, a CVD method etc., a tetra-ethoxy silane, etc., or the insulator layer which consists of those bipolar membrane, the photosensitive polyimide which is an organic material is applied and the protective coat 8 with a thickness of about 6 micrometers is formed by exposing, developing and hardening this. Thereby, a protective coat 8 is formed on the wafer 9 with which the semi-conductor was formed. Although thickness of a protective coat 8 was made into 6 micrometers in this example, necessary thickness changes with classes of the semiconductor device concerned, and the range becomes 1 thru/or about 10 micrometers. In addition, although it does not matter even if it is formed so that the whole surface may be covered mostly, of course, as shown in drawing 33 - drawing 35 , even if this organic film is formed only in the field of the inorganic film which becomes near the aluminum pad 7, it is not cared about as shown in drawing 13 . In the case of the insulator layer which consists only of an inorganic material, the range of thickness becomes 3 micrometers or less. Moreover, poly benzoxazole, poly benz-cyclo-butene, the poly quinoline, poly FOSUFAZEN, etc. can be used besides the photosensitive polyimide used in this application example.
[0025] The third process: Carry out printing spreading of the paste-like polyimide ingredient in the formation schedule part of the stress relaxation layer 5, and make it harden by heating this after that. Thereby, the stress

relaxation layer 5 is formed on a protective coat 8.
[0026] The fourth process: Use the reverse pattern 17 of wiring and form a photoresist, after forming the electric supply film 16 for using for electroplating by approaches, such as a spatter.
[0027] The fifth process: Perform electroplating using this electric supply film 16 and the reverse pattern 17 of wiring, and perform formation of the wiring 4 for rewiring, and the bump pad 3. Moreover, wiring 4 for rewiring is made into multilayer structure by repeating electroplating if needed.
[0028] The sixth process: Etching processing removes the reverse pattern 17 of wiring which consists of a photoresist, and the electric supply film 16 of electroplating.
[0029] The seventh process: Form the surface protective coat 6 using a solder resist. And non-electrolyzed gilding 2 is performed on the maximum front face of the bump pad 3 using this pattern.
[0030] The eighth process: On the bump pad 3, connect a solder ball to the bump pad 3 by carrying and heating a solder ball with flux, and form a bump 1.
[0031] The ninth process: A wafer dicing technique cuts the wafer 9 with which the semi-conductor was formed to a semiconductor device 13.
[0032] Below, it attaches by the eighth process from the third above-mentioned process, and explains to a detail.
[0033] First, the third process is explained. The mask used for printing has the usable thing of the same structure as the mask for printing used by soldering paste printing to a printed wired board etc. For example, as shown in drawing 6 , the metal mask of the gestalt which stuck the stencil 25 made from a nickel alloy on the frame 27 through the resin sheet 26 can be used. Since a paste is damp and about 50 micrometers of pattern openings 28 o the mask for printing spread after printing, you may make it manufacture them the part and smallness which expected it. As shown in drawing 7 , it is that paste printing sticks the mask for printing, and the pattern of the wafer 9 with which the semi-conductor was formed where alignment is carried out, and a squeegee moves in the condition in a stencil 25 top, and is filled up with the pattern opening 28, and it is raising the mask for printing relatively after that to the wafer 9 with which the semi-conductor's was formed, and the so-called contact printin which prints is performed. In addition, adhesion of the wafer said here and the mask for printing does not necessarily mean completely losing a clearance among both. Since the protective coat 8 is already partially formed on the wafer, it is because it is difficult practically to stick a printing mask without a clearance on this. A this example, it printed on printing conditions from which the clearance between a wafer and the mask for printing becomes 0-100 micrometers. In addition, the whole squeegee side of the mask for printing is coated wit the first squeegee with a paste, the pattern opening 28 of the mask for printing is filled up with the second squeegee after that, and an excessive paste is removed. Then, there is also the printing approach of raising the mask for printing relatively to the wafer 9 with which the semi-conductor was formed. You may make it go up, although you may make it go up perpendicularly as shown in drawing 8 in case a printing mask is relatively raised to a wafer 9, moving so that it may have a tilt angle relatively. By giving a tilt angle, a version detached building angle in case a printing mask separates from a wafer tends to become homogeneity in a wafer side. Moreover, the printing mask will separate from one edge of a wafer toward the other end, at the moment of the last of a version detached building when a version omission tends to become unstable, will be performed in a field without a semiconductor device, and becomes advantageous also in respect of the improvement in the yield Furthermore, when performing continuous printing to two or more sheet wafer using the same printing machine, it is good to insert the process which wipes the background of the mask version with proper timing. For example in this example, when ten-sheet continuation printing was carried out, the background of the mask version was cleaned once, and printing of the 11th sheet was performed after an appropriate time. As for the timing of cleaning of a mask background, a count, and its approach, accommodation is needed suitably with the viscosity and solid content concentration of a paste ingredient, the amount of fillers, etc.
[0034] A paste hardens by heating gradually the wafer 9 with which the semi-conductor with which printing spreading of the paste was carried out succeedingly was formed using a hot plate or a heating furnace, and formation of the stress relaxation layer 5 is completed.
[0035] The ingredient for formation of the stress relaxation layer 5 currently used here is paste-like polyimide, and can be hardened by heating, after printing spreading is carried out on a protective coat 8. Moreover, the polyimide of the shape of this paste consists of a minute particle of the polyimide of a large number distributed the precursor of polyimide, a solvent, and in it. As a particle, it is specifically mean particle diameter 1 thru/or 2

micrometers, and the minute particle which has the particle size distribution from which a maximum grain size becomes about 10 micrometers was used. Since the precursor of the polyimide used for this example will serve a the same ingredient as the minute particle of polyimide if it is hardened, when paste-like polyimide hardens, the uniform stress relaxation layer 5 which consists of one kind of ingredient will be formed. Although polyimide was used as a stress relaxation stratification ingredient in this example, it is also possible in this example to use amide imide resin, ester imide resin, ether imide resin, silicone resin, acrylic resin, polyester resin, the resin that denaturalized these in addition to polyimide. When using resin other than polyimide, it is desirable to give conversion to a resin presentation so that processing which gives compatibility to the above-mentioned polyimid minute particle front face may be performed or compatibility with the above-mentioned polyimide minute particle may be improved. In the resin which has imide association among the resin which carried out [above-mentioned] listing, for example, polyimide, amide imide, ester imide, and ether imide, it excels in a heat mechanical property, for example, the reinforcement in an elevated temperature etc., thanks to the firm frame by imide association, and ****** of the plating electric supply film formation approach for wiring spreads as the result. For example, the plating electric supply film formation approach accompanied by high temperature processing, such as a spatter, can be chosen. When it is resin with the part condensed in association other than imide association, such as silicone resin, acrylic resin, polyester resin, amide imide, ester imide, and ether imide, although a heat mechanical characteristic is inferior a little, it may be advantageous in respect of workability, a resin price, etc. For example, by polyester imide resin, generally, since curing temperature is lower than polyimide, it is easy to treat. In this example, a component property, a price, a heat mechanical characteristic, etc are synthetically taken into consideration out of these resin, and these resin is used properly suitably.

[0036] Since it becomes possible to adjust the visco-elastic property of an ingredient by distributing a polyimide minute particle into paste-like polyimide, the paste excellent in printing nature can be used. Since it becomes possible to control the thixotropy property of a paste by adjusting combination of a minute particle, a printing property is improvable by combining with adjustment of viscosity. Moreover, whenever [tilt-angle / of the stress relaxation layer 5] can also be adjusted. It is desirable for the suitable thixotropy property of a paste to have the so-called thixotropy index for which it asked from the ratio of the viscosity in engine-speed 1rpm measured using the rotational viscometer and the viscosity in engine-speed 10rpm in the range of 2.0 to 3.0 in this application example. In addition, when it is the paste with which temperature dependence appears in a thixotropy index, high results will be acquired if it prints in a temperature field in which a thixotropy index becomes the range of 2.0 to 3.0.

[0037] After carrying out heat hardening of the polyimide of the shape of a printed paste, the stress relaxation layer 5 which has a cross-section configuration as shown on the wafer 9 at drawing 9 is formed. Thus, although i may swell at the place of 200 thru/or 1000 micrometers and a part may exist from the edge section of the stress relaxation layer 5 if the stress relaxation layer 5 is formed by printing, about the location of this swelling part, and the existence of existence, the presentation of paste-like polyimide is adjusted, or it is changing the various conditions in connection with printing, and becomes to some extent controllable. In addition, as various conditions in connection with printing in this case, **, such as metal mask thickness, a squeegee rate, the squeegee quality of the material, a squeegee include angle, squeegee ** (printing pressure), a version detached building rate, temperature of the wafer at the time of printing, and humidity of a printing environment, are raised Although the above-mentioned printing conditions can attain control of the height of the above-mentioned swelling part, or a configuration, there is also an approach by the structural adjustment of a protective layer 8 as the other control approaches. For example, if the formation field of the organic layer of a protective coat 8 is limited only near the pad 7 as shown in drawing 36 , it is easy to make the stress relaxation layer of the part equivalent to the organic layer upper part heaped up.

[0038] Moreover, as shown in drawing 1 , when it swells in the stress relaxation layer 5 and a part is formed positively, the deflection part of wiring 4 can be formed, it becomes the structure which is easy to absorb the stress by thermal expansion etc. by this, and an open circuit can be prevented more. It is desirable that about 25 micrometers of swelling parts which have 7 thru/or height of about 12 micrometers desirably are specifically formed at the maximum to the average thickness of the stress relaxation layer 5. If it is top-most vertices of this level, it can form enough by mask printing. For example, if a radius assumes this swelling section to be the shape of a semi-cylindrical shape which is 10 micrometers, the die length of the half-arc of the swelling section

becomes (2x3.14x10 micrometers) / 2= 31.4 micrometers, and the redundancy die length of wiring will become 42.8 micrometers when it forms in every one both sides of 31.4-10=21.4 micrometer and a stress relaxation layer about the one swelling section. Thus, since the redundancy section can be prepared in wiring 4, the thermal stress which acts on wiring structure and the soldered joint section is eased, therefore reliable wiring structure can be offered. In addition, it asks for the necessary thickness of this swelling section from the experiment and simulation which took into consideration the thickness of the stress relaxation layer 5 and an elastic modulus, the size of a semiconductor device 13, the power consumption of a semiconductor device, the physical-properties value of the circuit board 14 in which a semiconductor device is carried, etc. For example, in this example, the diagonal die length of a semiconductor device 13 is made into L millimeters. If the maximum temperature requirement which the difference of the coefficient of linear expansion of the circuit board 14 in which a semiconductor device 13 and it are carried produces by ON/OFF under the substrate loading process of 15 ppm [degree C] /and a semiconductor device 13 - actuation carries out to 200-degree Centigrade The maximum heat deformation which the wiring section receives [a substrate mounting article] by use by the real operating environment becomes 15(ppm/degree C) xL/2(mm) x200 (degree-C) =0.0015xL millimeter. Therefore, when there were about 0.002xL millimeters of redundancy die length required of the above-mentioned swelling section, I thought that it was enough. It swells from this count, the section is approximated by the shape of a semi-cylindrical shape, and it was made for the height of that swelling part to be settled in L / the range of about 2000 - L/500 millimeter to the average thickness of the stress relaxation layer 5 in this example.

[0039] When the thickness of the needed stress relaxation layer 5 is not formed by one printing and heat hardening, thickness predetermined by repeating printing and hardening of an ingredient two or more times can be obtained. For example, when a metal mask with a thickness of 65 micrometers is used using the solid content concentration 30 thru/or 40% of paste, about 50 micrometers can be obtained as thickness after hardening by two printings. Moreover, especially about the bump 1 stationed in the part which distortion tends to concentrate when a semiconductor device 13 is connected to the circuit board 14, concentration of distortion can also be eased by limiting only to the stress relaxation layer 5 of the corresponding part, and thick-film-izing thickness. for this reason -- being alike -- for example, what is necessary is just to print multiple times using a different metal mask from what used paste-like polyimide by the 1st printing to the wafer 9 top with which the semi-conductor was formed Moreover, the thickness of a stress relaxation layer can also be partially changed by adjusting the structure of a protective layer 8 as the 2nd approach. For example, as shown in drawing 37 , Bump's X field [directly under] which a strain tends to concentrate uses only the protective layer which consists of inorganic film, and uses as a protective coat the compound layer in which the organic film was formed on the inorganic film, in other fields. If a stress relaxation layer is formed on such a protective coat, a loose ramp will be formed in the parts A of a place with the protective coat of the organic film, and the stress relaxation layer which is not. Now, for the thickness of 1GPa and the organic film, in 10 micrometers, the average elastic modulus (GPa/micrometer) of the part which will consist of an organic protective coat and a stress relaxation layer supposing it is 3GPa(s) is set to (3x10+1x50) / 60**1.3, and, on the other hand, the thickness of a stress relaxation layer of the average elastic modulus of the ramp in Part A is [the elastic modulus / the elastic modulus] 1 at 50 micrometers. Therefore, with such structure, it will distribute into the part in which the organic protective coat was formed from the periphery, and the thermal stress of a stress relaxation layer can prevent breakage of the bump in the periphery which thermal stress originally concentrates. In addition, it is not necessary to necessarily have a particle in a stress relaxation layer, and even when not distributing a particle during a paste, minimum viscoelastic property required for printing should just be secured. However, when not distributing a minute particle during a paste, the margin of the various conditions in connection with printing may become extremely narrow.

[0040] The fourth process is explained succeedingly. In this example, wiring 4 for rewiring was made two-layer [of electrolytic copper plating and electric nickel]. In addition, the end of the wiring 4 for rewiring may be used also [pad / 3 / bump]. Although here showed how copper and nickel form a conductor using electroplating, it is also possible to use nonelectrolytic plating.

[0041] First, the electric supply film 16 for carrying out electroplating is formed all over a semiconductor wafer. Here, although it was possible to have used vacuum evaporationo, non-electrolytic copper plating, CVD, etc., the bond strength with a protective layer 8 and the stress relaxation layer 5 decided to use a strong spatter. As

pretreatment of a spatter, in order to secure the flow between a bonding pad 7 and wiring 4 conductor for rewiring, sputter etching was performed. As spatter film in this example, the multilayers of chromium (75 nanometers)/copper (0.5 micrometers) were formed. The function of chromium here is to secure adhesion of the copper, stress relaxation layer, etc. which are located up and down, and the thickness has the desirable minimum which maintains those adhesion. When chromium thickness becomes thick, membrane formation time amount will increase, in addition to the problem that productive efficiency falls, a protective layer 8 and the stress relaxation layer 5 will be put to the plasma of the high energy condition generated in a spatter chamber over long duration, and there is a danger that the ingredient which forms these layers will deteriorate. In addition, although necessary thickness is changed by the conditions of sputter etching and a spatter, the membraneous quality of chromium, etc., it is 0.5 micrometers at the maximum in general. In addition, it replaces with the chromium film used by this example, and the titanium film, titanium / platinum film, and a tungsten can also be substituted. On the other hand, when the electrolytic copper plating and electric nickel plating which are performed at a next process are performed, the minimum thickness of the thickness of spatter copper which thickness distribution of the plating film does not produce is desirable, and it determines the thickness which does not induce thickness distribution after also taking into consideration the amount of film decreases in acid washing performed as plating pretreatment. In the case of the copper thickness exceeding 1 micrometer, when thickness of spatter copper is made thick beyond the need, spatter time amount becomes long, in addition to the problem that productive efficiency falls, long duration etching is not avoided in the case of etching removal of the electric supply film 16 carried out at a next process, but side etching of the wiring 4 for rewiring becomes large as the result. By simple count, in etching the 1-micrometer electric supply film, also in wiring, 2-micrometer etching takes place on 1 micrometer of one side, and both sides. In actual production, since carrying out over etching is generally performed so that the etching remainder of the electric supply film may not occur, when etching the 1-micrometer electric supply film, side etching of about 5 micrometers of the wiring will be carried out. If side etching becomes large in this way, wiring resistance becomes large, or it will become easy to induce an open circuit and will be easy to generate a problem in the viewpoint of the wiring engine performance. Therefore, the thickness of spatter copper becomes 1 micrometer at the maximum in general.

[0042] Next, the reverse pattern configuration 17 of the wiring 4 for rewiring is formed using a resist using a phc lithography techniques. The thickness of the resist in the edge section of the stress relaxation layer 5 shown by B in drawing 4 becomes thick by the resist which flowed out of the slant surface part compared with other locations. For this reason, the negative mold is more desirable in order to secure resolution. As a resist, when a liquefied resist is used, resist thickness tends to become thin and there is an inclination for resist thickness to ten to become thick conversely, in the slant-face lower part in the slant-face upper part of the edge section of the stress relaxation layer 5 shown by B in drawing 4 . Large development tolerance is needed for carrying out patterning of the resist from which thickness differs in the slant-face upper part and the slant-face lower part on the same same light exposure and development conditions. Generally, since the negative-mold sensitization property resist was larger than a positive type sensitization property resist, the development tolerance to thickne used the liquefied resist of a negative mold in this example. In addition, in using a film resist, since it does not generate, ****** in the slant-face upper and lower sides becomes usable also with a negative mold or a positive type, but since a slant surface part will be exposed from across and the real optical path length becomes long, if a negative mold is used also in this case, good results will be obtained in many cases. A negative mold is desirable especially when using a film resist with weak case where the inclination of the edge section of the stress relaxation layer 5 is large and breeching property. In this example, as shown in drawing 10 , the exposure mask 21 and the resist 22 stuck and the exposure machine of the type which has a clearance 20 in a part was used. The resolution limit in this exposure machine was about 10 micrometers in the case where the mask 21 for exposure and a resist 22 stick. According to our experimental result, the clearance 20 between the exposure mask 21 lowe parts and the relation of the wiring width of face to resolve came to be shown in Table 1. In addition, the value ir Table 1 changes with the ratios of the optical system and the development conditions of an exposure machine, th sensibility of a resist, resist hardening conditions, and wiring width of face / wiring spacing etc. The experimenta result shown in Table 1 is a value in case the ratio of wiring width of face / wiring spacing is 1.0.

[0043]

[Table 1]

表 1

		露光マスク下部の隙間 [μm]			
		40	60	80	100
配線幅 [μm]	15	×	×	×	×
	20	○	×	×	×
	25	○	○	○	×
	30	○	○	○	○
	40	○	○	○	○
	50	○	○	○	○

○：解像可
×：解像不可

[0044] Signs that a connection 23 and the bump putt 3 with an aluminum pad are connected to drawing 11 with the wiring 4 for rewiring are shown. In the case of the aligner used by this example, since the clearance between the lower parts of the exposure mask which is the axis of abscissa of Table 1 supports the thickness of a stress relaxation layer mostly, if the thickness of a stress relaxation layer is 60 micrometers, for example, the width of face of wiring is resolvable to 25 micrometers. Therefore, wiring width of face of a signal line can be made into 25 micrometers, and it can also wire by making wiring width of face of a power source or a grand line into 40 micrometers. Moreover, it is also possible to make thick a part of the signal line, using wiring of a signal line as 25 micrometers.

[0045] The wiring 4 for rewiring in near the ramp of the stress relaxation layer 5 is expanded and shown in drawing 12 . As mentioned above, since resist thickness served as an ununiformity near the edge section of the stress relaxation layer 5, there was an inclination which a underdevelopment tends to generate in the field. Signs that the underdevelopment has actually happened to drawing 13 in the edge part of the stress relaxation layer 5 are shown. In this example, it solved by improving a surroundings lump of a developer for this cure. When it illustrates more concretely, they are policies, such as changing a circuit pattern configuration, as shown in drawing 14 or drawing 15 .

[0046] Drawing 14 shows the case where drawing 15 makes thick wiring width of face of only the edge part of the stress relaxation layer 5 with bad definition for the case where wiring width of face is made thick from the connection 23 with an aluminum pad to near the summit of the stress relaxation layer 5. In addition, the wiring width of face in these drawing 14 and drawing 15 is determined in consideration of the resolving property shown in the thickness and Table 1 of the stress relaxation layer 5. How to cancel the development remainder by extending developing time as other solutions is also considered. Moreover, since light diffracts in respect of a mask, it may originate in a clearance 20 existing under the exposure mask 21, and a definition fall and a pattern precision fall may take place.

[0047] As a solution of this phenomenon, optical-system modification of (1) exposure machine, breeching nature amelioration of (2) resists, prebaking condition rationalization of (3) resists, (4) multistage exposure, etc. are raised. If one example is given about modification of the optical system of an exposure machine, the policy that NA value uses 0.2 or less or more 0.0001 exposure machine will be raised. The definition of a pattern and precision can be improved by combining suitably the device on the process of not only the example given here but well-known common use.

[0048] Since the edge section of the stress relaxation layer 5 has the description on the structure which the stress produced by the difference in the physical-properties value of a wafer and the stress relaxation layer 5 tends to concentrate, an open circuit can also be effectively prevented by making wiring thick by the ramp of the stress relaxation layer 5. In addition, you may make it change the width of face of wiring with a power source / grand line, and a signal line, as it is necessary to not necessarily make no wiring into the same size for example, and is shown in drawing 16 . In this case, when an electric property is taken into consideration, it is desirable to make a power source / grand line thicker than a signal line generally. It is because the capacity component which wiring

has by this increases and effect is done at the time of high-speed operation, when a signal line is made thick. Conversely, since the effectiveness that supply voltage is stabilized is expectable if a power source / grand line is made thick, it is desirable rather. Therefore, it is desirable to consider as the pattern which made the edge circumference thick so that it may illustrate, and only the part which stress concentrates can be eased at worst about wiring for signals, and to make a ramp thick uniformly about wiring for the object for power sources or glands. On the other hand, about the flat part in which the stress relaxation layer is not formed, signal wiring is made thin in consideration of the effect of the capacity component of wiring. However, it is necessary to take thi into consideration with the class of semiconductor device, or its circuit pattern each time. For example, although it is dependent also on a semiconductor device or its circuit pattern, since big effectiveness is in capacity reduction of wiring when the thickness of a protective coat 8 is increased, when signal wiring must be made thicl by the flat part in which the stress relaxation layer is not formed, it is desirable to form a protective coat 8 thickly When increasing wiring width of face 10%, specifically, it is desirable to also increase the thickness of a protective coat 8 about 10%. On the other hand, the wiring width of face in the up flat part of a stress relaxation layer receives a limit from signal-line capacity with a wiring consistency rather. That is, the upper limit of the wiring width of face in the up flat part of a stress relaxation layer is calculated from the alignment accuracy in th path of the wiring number which it lets pass at spacing of a bump pad, and a bump pad, and a wiring formation process etc. If an example is shown concretely, when bump pad spacing will pull 3 wiring between 300 micrometers of diameters of a pad, and a pad by 0.5 millimeters, it is (500-300) / (3x2-1) =40. It becomes the count to say. From this count result, they could be average wiring width of face / wiring spacing =40 micrometer by this example.

[0049] The fifth process is explained. In this example, copper plating was carried out using sulfuric-acid acidity copper-plating liquid. After electrolytic copper plating performed washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing, it connected the electric supply film 16 to cathode, and connected and carrie out the copper plate containing Lynn to the anode plate.

[0050] Then, electric nickel plating is performed. In addition, when washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing are performed before electric nickel plating, there is an inclination for the electric nickel-plating film of good membraneous quality to be easy to be obtained. Electric nickel plating connected the electric supply film 16 to cathode, connected the nickel plate to the anode plate, and went. Although the nickel-plating bath of the gap which is not well-known common use of electric nickel plating suitable at this example could also be usable and the Watts bath system or the sulfamine bath system was sufficient as it, it was performed using the Watts bath system under the plating conditions adjusted so that plating film internal stress might become the proper range by this example. Although there is a fault that a sulfamine bath has the inclination which a plating liquid component tends to decompose a little an expensive top compared with a Watts bath, coat stress tends to control it. On the other hand, since coat stress generally tends to become large, a Watts bath has the fault that the danger that a crack will go into a wiring layer for the coat stress (tensile stress) which self has increases, when thick-film plating is carried out. Although the Watts bath was used in this example, when using a sulfamine bath, or when using a Watts bath, it is good to carry out, after carrying out beforehand the model experiment for asking for the proper range of whenever [class / of additive (coat stress inhibitor) / and concentration, plating current density, and plating solution temperature]. It carried out, after searching for beforehand the conditions from which these are controlled by this example proper, and a crack doe not go into wiring in 10 micrometers or less of thickness. In addition, plating membrane stress is one of the indexes in connection with the metallic crystal stacking tendency of depositing nickel, and in order to control growth of the solder diffusion layer mentioned later, it is necessary to control it proper. If membrane stress galvanizes under the conditions controlled proper, a plating coat will come to carry out the cutectoid of the mino constituent of the amount of specification. For example, in the case of the film containing 0.001 - 0.05% of sulfur, the content of a specific crystal orientation side increases. Speaking more concretely, the content sum tota of the orientation sides 111, 220, and 200 and 311** becoming 50% or more. The thickness of electric nickel plating determines an optimum value with the class and reflow conditions of the solder used at a subsequent process, and the product property (mounting gestalt) of a semiconductor device. What is necessary is just to determine that the thickness of the alloy layer of the solder and nickel which are formed in the case of a solder reflow or mounting repair will specifically become more than nickel-plating thickness. The thickness of the

above-mentioned alloy layer becomes so large [it is so large that the concentration of the tin in solder is high, and] that reflow upper limit temperature is high. Thus, when the nickel layer was formed after copper wiring as wiring for rewiring, wiring for rewiring receives deformation with the thermal stress committed between a semiconductor device and the circuit board and the stress is released after that, wiring for rewiring can return to the configuration before deformation by the spring nature of a nickel layer. For example, it deforms in the form which the wiring 4 for rewiring currently formed a stress relaxation layer and on it stuck to each other according to an operation of the thermal stress caused by actuation of a semiconductor device. The deflection part of the redundancy part of wiring for rewiring in the swelling part of a stress relaxation layer is used for deformation of wiring for rewiring at this time. Then, when it is released from thermal stress etc. and a stress relaxation layer returns to the original configuration, for wiring for rewiring, only in copper wiring, copper wiring is a pile to return in the original wiring configuration at own spring nature of copper wiring. On the other hand, if a nickel layer is formed after copper wiring, wiring for rewiring (copper wiring) can return to the original configuration easily by the spring nature of the nickel layer. In addition, being formed after copper wiring may have spring nature comparable as a nickel layer not only on a nickel layer but on copper wiring. Moreover, to form wiring which is elastic instead of copper wiring, a nickel layer is necessarily unnecessary.

[0051] At the sixth process, after performing electrolytic copper plating and electric nickel plating, the resist 17 which is the reverse pattern of wiring is removed, and the electric supply film 16 which formed membranes beforehand by carrying out etching processing is removed. Although there was a class of ferric chloride, alkali system etching reagent, etc. of copper etching, in this example, the etching reagent which uses a sulfuric acid/hydrogen peroxide solution as a principal component was used. If there is no etching time for 10 seconds or more, control will become difficult, and since it will also produce the problem that side etching becomes large or a baton becomes long in etching, for example exceeding 5 minutes if too much long time amount etching is performed although it is disadvantageous in a practical viewpoint, an etching reagent and etching conditions are good to ask by experiment suitably. By this example, the etching reagent which uses potassium permanganate and a meta-silicic acid as a principal component was used for etching of the chromium part of the electric supply film 16 carried out succeedingly. In addition, the above-mentioned electric nickel-plating film is functioning also as etching resist in the case of etching of the electric supply film 16. Therefore, it is good to take into consideration the etch selectivity of nickel, copper and nickel, and chromium, and to determine the presentation component of an etching reagent, and etching conditions. For example, speaking concretely, by the sulfuric-acid hydrogen-peroxide etching agent used in the case of copper etching, making the content of a sulfuric acid into 15% or less desirably 50% or less at the maximum. Thereby, copper can be etched by about 10-time etch selectivity to nickel.

[0052] At the seventh process, only the bump pad 3, the cutting section 24, and its perimeter formed the surface protective coat 6 which carried out opening, and formed gold in the bump pad section 3 by carrying out non-electrolyzed gilding succeedingly. Here, after using a solder resist as a surface protective coat 6 and applying this all over a semiconductor device 13, a pattern is formed in exposing and developing negatives. In addition, it is also possible to use ingredients other than a solder resist, such as photosensitive polyimide and polyimide for printing, and to form the surface protective coat 6. By passing through the above processes, the surface protective coat 6 will cover completely the wiring 4 for rewiring, the stress relaxation layer 5, a protective coat 8, etc. For this reason, the surface protective coat 6 can inhibit that the wiring 4 for rewiring, the stress relaxation layer 5, and a protective coat 8 deteriorate, exfoliate and corrode with the stimulative matter.

[0053] Even at this seventh process, the wiring 4 for rewiring from the aluminum pad 7 to the bump pad 3 and the bump pad 3 are formed, as shown on the wafer 9 with which the semi-conductor was formed at drawing 17 and drawing 2 .

[0054] At the eighth process, a bump is formed using solder ball loading equipment and a reflow furnace. That is, the flux and the solder ball of the specified quantity are carried on the bump pad 3 by using solder ball loading equipment. Under the present circumstances, temporary immobilization of the solder ball is carried out by the adhesion of flux on a bump pad. It is once fusing a solder ball and solidifying again after that in throwing into a reflow furnace the semiconductor wafer with which the solder ball was carried, and becomes the bump 1 linked to the bump pad 3 shown in drawing 1 . In addition, there is also the approach of forming a bump 1 by carrying out printing spreading of the soldering paste on the bump pad 3 using a printing machine, and carrying out a

reflow of this. Also in which approach, it becomes possible [a solder ingredient] to choose various things, and many of solder ingredients currently supplied to the commercial scene in this time can be used. In addition, although a solder ingredient is limited, it is using a plating technique and there is also the approach of forming a bump 1. Moreover, the bump who formed using the resin which blended the bump who used the ball which used gold and copper as the nucleus, and the electrical conducting material may be used.

[0055] By passing through the process from the first process to the ninth process, it has the stress relaxation laye 5 shown in drawing 1 , and the wiring 4 for rewiring is formed by the small routing counter, and the semiconductor device 13 with which the flection which stress moreover concentrates in the middle of the wiring 4 for rewiring does not exist can be realized. Moreover, pattern formation of the stress relaxation layer 5 which i an insulating layer of a thick film can be carried out by using a printing technique, without using exposure and a development technique, and the stress relaxation layer 5 can have a slant face for forming the wiring 4 for rewiring.

[0056] According to this example, even when under-filling is not carried out but flip chip bonding of the semiconductor device 13 is carried out, the connection dependability of a semiconductor device 13 improves sharply. For this reason, it turns out that the flip chip bonding which does not use under-filling in many electric products becomes possible according to this example, and it becomes possible to reduce the prices of various electric products. Furthermore, since under-filling is not carried out, removal of a semiconductor device 13 is attained. That is, when the semiconductor device 13 linked to the circuit board is a defective, it becomes possible to remove a semiconductor device 13 from on the circuit board, and to reproduce the circuit board, and it becomes possible to reduce the prices of various electric products also by this.

[0057] Next, the ingredient of the stress relaxation layer 5 concerning this example is explained. Although the ingredient for stress relaxation layer 5 formation used most suitably at this example is paste-like polyimide, not only this but conversion amide imide resin, ester imide resin, ether imide resin, polyester resin, conversion silicone resin, conversion acrylic resin, etc. are sufficient as it. In the resin which has imide association among the resin which carried out [above-mentioned] listing, for example, polyimide, amide imide, ester imide, and ether imide, it excels in a heat mechanical property, for example, the reinforcement in an elevated temperature etc., thanks to the firm frame by imide association, and ****** of the plating electric supply film formation approach for wiring spreads as the result. For example, the plating electric supply film formation approach accompanied by high temperature processing, such as a spatter, can be chosen. When it is resin with the part condensed in association other than imide association, such as silicone resin, acrylic resin, polyester resin, amide imide, ester imide, and ether imide, although a heat mechanical characteristic is inferior a little, it may be advantageous in respect of workability, a resin price, etc. For example, by polyester imide resin, generally, since curing temperature is lower than polyimide, it is easy to treat. In this example, a component property, a price, a heat mechanical characteristic, etc. are synthetically taken into consideration out of these resin, and these resin is used properly suitably. Two or more kinds are blended, a coupling agent, a coloring agent, etc. for improving an adhesive property with various interfaces to this are blended, and the ingredient for stress relaxation layer 5 formation can use [independent or] resin, such as epoxy, a phenol, polyimide, and silicone.

[0058] Although the elastic modulus of the stress relaxation layer 5 can apply the thing of 0.1 to 10.0GPa extent in a room temperature, what has an elastic modulus lower than common polyimide is desirable. In being too small, in case it performs the formation of a projection electrode and the functional test of this semiconductor device which are mentioned later by an elastic modulus being less than 0.1GPa(s), we become easy to deform a wiring part and are anxious about problems, such as an open circuit. Moreover, if the elastic modulus of the stres relaxation layer 5 becomes large exceeding 10.0G, the reduction effectiveness of sufficient stress will not be acquired, but we are anxious about the connection dependability at the time of carrying this semiconductor device in a substrate falling.

[0059] Furthermore, as for the curing temperature of the charge of stress relaxation layer 5 material, it is desirable to use the thing from 100 degrees C to 250 degrees C. It is because wafer stress increases by the heat shrink at the time of hardening cooling or there is concern from which the property of a semiconductor device changes, when management within the process at the time of semi-conductor manufacture is difficult and curing temperature becomes high from this when curing temperature is lower than this. Since the stress relaxation layer after hardening is exposed to various processes, such as a spatter, plating, and etching, properties, such as therma

resistance, chemical resistance, and solvent resistance, are also required. concrete -- as thermal resistance -- the glass-transition temperature (Tg) -- 150 degrees C -- super- -- it is desirable that it is 400 degrees C or less, and Tg is [180 degree C or more of Tg(s)] 200 degrees C or more most preferably more desirably. Drawing 41 is an experimental result which shows the relation between glass transition temperature (Tg) and coefficient of linear expansion. This shows that the crack has not occurred, if glass transition temperature (Tg) is 200 degrees C or more. In addition, the coefficient of linear expansion (alpha 1) in the field below [the viewpoint which stops the deformation in various temperature processings in a process to] Tg is so desirable that it is small. It is so good that it is specifically close to 3 ppm. Although a low spring material generally has a large coefficient of linear expansion in many cases, as for the range of the coefficient of linear expansion of stress relaxation layer 5 ingredient suitable at this example, it is desirable that it is the range of 3 ppm - 300 ppm. It is the range of 3 ppm - 200 ppm more preferably, and the range of the most desirable coefficient of linear expansion is 3 ppm - 150 ppm. On the other hand, as for pyrolysis temperature (Td), it is desirable that it is about 300 degrees C or more. When Tg and Td are less than these values, there is a danger that deformation of resin, and deterioration and decomposition will take place at a spatter or a sputtering etch process as the heat process in the inside of a process. When it says from a chemical-resistant viewpoint, it is desirable for resin deterioration of discoloration, deformation, etc. not to take place 30% by the immersion of 24 hours or more to a sulfuric-acid water solution oi 10% sodium-hydroxide water solution. As solvent resistance, it is desirable to set a solubility parameter (SP value) to 8-20(cal/cm3) 1/2. When the object for the stress relaxation layers 5 is the ingredient which comes to carry out conversion of some components to base resin, it is desirable for the greater part of the presentation to have said the range of the above-mentioned solubility parameter. Speaking more concretely, it being desirable fo less than 8 and a 20 super-****** component not to contain [the solubility parameter (SP value)] more than 50 % of the weight. When such chemical resistance and solvent resistance are insufficient, an applicable manufacture process may be limited and it is not sometimes desirable from a viewpoint of manufacturing cost reduction. After taking into consideration synthetically actually the ingredient cost and the process degree of freedom with which are satisfied of these properties, it is good to determine the ingredient for stress relaxation layer 5.

[0060] Then, the relation between the thickness of a stress relaxation layer, wafer stress, and alpha rays is explained. Drawing 18 shows the thickness of a stress relaxation layer, and the relation of wafer stress. When diameter the wafer of 8 inches is made to apply and harden a stress relaxation layer, if thickness becomes thick rather than 150 micrometers, wafer stress becomes large, and as shown in drawing 18 , the crack of a wafer, peeling of an insulator layer, etc. will become easy for the curvature of a wafer to become large or to generate it.

[0061] On the other hand, the relation between the thickness of a stress relaxation layer and the amount of alpha rays which penetrates the inside of a stress relaxation layer was shown in drawing 19 . It generates by collapse oi uranium, thorium, etc. which are contained as an impurity in the solder used for a semiconductor device, and alpha rays cause malfunction of the transistor section. If the thickness of a stress relaxation layer becomes thicke than 35 micrometers as shown in drawing 19 , alpha rays will hardly be penetrated, and the problem of malfunction by alpha rays is not produced. Since alpha rays will penetrate if the thickness of a stress relaxation layer becomes thin from 35 micrometers on the contrary, it turns out that malfunction by alpha rays becomes easy to take place.

[0062] Connection dependability with the substrate in which it prevented that alpha rays reached to the circuit part formed in the semiconductor device front face from these relation by making thickness of a stress relaxation layer into 35 micrometers or more 150 micrometers or less, and a semiconductor device and this were carried is securable. In addition, the part which cannot be easily influenced [the memory cell 110 grade which is easy to receive incorrect actuation of the part which is easy to be influenced of alpha rays depending on the configuratio: of a semiconductor device, for example, a transistor, and] of alpha rays is in the same component. Then, it can prevent that alpha rays reach to the circuit part formed in the semiconductor device front face by making thickness of a stress relaxation layer into 35 micrometers or more 150 micrometers or less to the part which is [as opposed to / especially / alpha rays] easy to be influenced, as shown in drawing 20 and 21. In addition, even if it makes it less [the thickness of the stress relaxation layer formed in the field which cannot be easily influenced of alpha rays] than 35 micrometers, it is satisfactory in the viewpoint of alpha-rays electric shielding. As it follows, for example, is shown in drawing 21 , alpha-rays electric shielding forms the stress relaxation laye

of a required field thickly, in other fields, a stress relaxation layer can be formed thinly, and average thickness of the whole stress relaxation layer can also be made into 35 micrometers or more 150 micrometers or less. When giving such a device, it is desirable to consider as the configuration of the semiconductor device which took into consideration the magnitude of the thermal stress strain concerning each bump. Since such a stress relaxation layer thicker [be easy to receive a thermal stress strain and] that it generally goes to the periphery of a semiconductor device 13 is needed, it is good to arrange the transistor field which is easy to be influenced to alpha rays on the periphery of a semiconductor device 13, and to arrange the field which cannot be easily influenced to alpha rays near the center of a semiconductor device 13. For example, as shown in drawing 38 , it i also possible to make thickness of the stress relaxation layer 5 so gradually thick [near the center of a semiconductor device 13 is thin, and] that it go to the periphery section. In this case, since a connection angle becomes small while connection height becomes large compared with other bumps, the bump's herself stress relaxation function increased and the bump near a center has substituted for the stress relaxation function of the stress relaxation layer 5 which became thin. In addition, as shown at drawing 39 in the case of the semiconductor device 13 which has the field which is not influenced at all of alpha rays, as long as it arranges the field which is not influenced of alpha rays near the center of a semiconductor device 13, the stress relaxation layer 5 may not b formed near the center of a semiconductor device 13. Next, the example of the stress relaxation layer which includes the particle from which a stress relaxation layer and a presentation differ as other examples is explained

[0063] The particle contained in the stress relaxation layer 5 mentioned above is the same ingredient as the stress relaxation layer 5, and has the same physical properties. It can have viscoelastic property required for printing because a particle distributes in a stress relaxation layer.
[0064] However, with this structure, since a physical-properties value changes rapidly on the boundary of a wafe and the stress relaxation layer 5, thermal stress etc. may concentrate on that boundary part, and wiring may carry out an open circuit etc.
[0065] Then, the property of the stress relaxation layer 5 formed on the circuit forming face of a wafer is change in the thickness direction, and it was made for the property of the stress relaxation layer by the side of a wafer front face to become close to the property of a wafer in this example.
[0066] The open-circuit prevention of the wiring section of the stress of the force discontinuous to wiring which lessened the difference of the property in the boundary section a wafer top face and under a stress relaxation layer, and established it on these by this, the tension by expansion contraction of a stress relaxation layer, or compression and bending is attained by making it not join the wiring section.
[0067] Furthermore, the substrate side with which the property of the stress relaxation layer 5 by the side of a wafer carries near and this semiconductor device in a wafer is effective not only in wiring on the stress relaxation layer 5 but the improvement in a connection life of the connection of this semiconductor device and said substrate by carrying out near to the property of the substrate.
[0068] Here, a coefficient of thermal expansion or an elastic modulus can be considered as a property of changing gradually in the thickness direction of the stress relaxation layer 5. And as a concrete means to change the property of a stress relaxation layer, as shown in drawing 22 , the silica particle 102 which is an insulating particle is blended, distribution of the loadings of the silica particle 102 is given in the thickness direction of the stress relaxation layer 5, and a coefficient of thermal expansion and an elastic modulus are changed gradually. In the part over which many silica particles 102 are distributed, an elastic modulus becomes [the coefficient of thermal expansion of the stress relaxation layer 5] small highly. On the other hand, if the loadings of the silica particle 102 decrease, a coefficient of thermal expansion will become large and an elastic modulus will become low.
[0069] By performing distribution of the circuit formation on a wafer, the stress relaxation stratification, and a silica particle, wiring formation on a stress relaxation layer, etc. in the state of a wafer, there are little simplification of a whole process, variation at the time of manufacture, etc., and the improvement in a life of the wiring section is possible also for the production process of the semiconductor device in this example.
[0070] In this example, one kind or the particle which blends two or more kinds and consists of organic materials, such as polyimide and silicone, if needed may be suitably blended for the particle which consists of inorganic materials, such as the silica and alumina which are an insulating particle for adjusting an elastic

modulus and heat expansion to the stress relaxation layer 5, and boron nitride.
[0071] Furthermore, since malfunction by the ultraviolet rays of the circuit section formed on modifiers, such as thermoplastics which raises the elongation after fracture and the breaking strength of the coupling agent and the resin which consists of alkoxysilane, titanate, etc. for adhesive improvement with the various interfaces which constitute a silica particle and an insulating resin layer, and a wafer etc. prevents, it is possible to also blend the hardening accelerator for promoting the hardening reaction of the color for coloring an insulating resin layer, a pigment, and a resin layer etc.
[0072] As the formation approach of the stress relaxation layer 5 of having changed the property in the thickness direction, the liquefied stress relaxation layer 5 which comes to blend the ingredient of said publication, for example is applied on the circuit side of a wafer, it is the process which carries out heat hardening of this stress relaxation layer 5, and there is a method of make the insulating particle which consists of a blended silica sediment gradually to a wafer side. If a particle with smaller particle diameter cannot sediment easily early, sedimentation turns a wafer down and a particle with larger particle diameter performs heat hardening of a stress relaxation layer when the particle diameter of a silica particle has distribution, distribution of a property will be formed in the thickness direction of a stress relaxation layer.
[0073] As an approach of controlling concentration distribution in the direction of thickness of the silica particle blended with the stress relaxation layer 5, the curing temperature of insulating resin and a curing temperature profile are adjusted suitably, or there is a method of changing the particle size distribution of insulating particles, such as an approach, a silica particle, etc. which blend suitably the reaction inhibitor for delaying the loadings of the hardening accelerator for bringing advance of hardening forward, a class, or hardening etc.
[0074] A silica particle applicable to this example can apply what fused and crushed the lump of the ingot-ized silica, the thing which carried out heating fusion and conglobated the silica particle again after crushing a silica ingot, the silica particle compounded further. The particle size distribution and loadings of a silica particle can be variously changed according to the magnitude of the semiconductor device which applies the structure of this example, thickness, a degree of integration, the thickness of the stress relaxation layer 5, and the particle size of a particle and the class of substrate to carry.
[0075] When forming the stress relaxation layer 5 by print processes, it may be necessary to change distribution of particle diameter also with the dimension of the mask applied depending on the approach of printing.
[0076] In addition, the stress relaxation layer 5 does not need to be formed by one printing, and as shown in drawing 23 , it may be formed by at least two printings or more. Furthermore, the loadings of the silica particle contained in each layer are changed, and you may print.
[0077] In this example, since the physical properties of the part in which wiring is formed do not change from the circuit section of a wafer rapidly in the phase of resulting in the electrode prepared on the stress relaxation layer, the big force does not concentrate on some wiring and open-circuit prevention of wiring is attained.
[0078] Next, an example of the example of the semiconductor device 13 which made thin thickness of the stress relaxation layer 5 of bump 1 directly under which exists in the circumference approach of a semiconductor device 13 compared with other parts is explained using drawing 24 . As for bump 1a of the outermost periphery, only in delta, in this example, height is low compared with bump 1b of that one inside.
[0079] There is a method of changing the rate of the solvent under printing conditions, such as existence of the minute particle contained in stress relaxation stratification ingredients, such as a paste-like polyimide ingredient, a configuration of a particle, combination and a print speed, a version detached building rate, and a count of printing, and paste etc. as an approach of making thickness of the stress relaxation layer 5 thin about the periphery of a semiconductor device 13.
[0080] In bump 1a which generally exists in the circumference approach of a semiconductor device 13, a big distortion has arisen compared with other bump 1b etc. with the various loads after connecting a semiconductor device 13 to the circuit board 14. For example, since the coefficient of linear expansion of a semiconductor device 13 and the circuit board 14 differs, at the time of a temperature rise, such a big distortion generates them that it is set to bump 1a of the circumference approach of a semiconductor device 13. When this distortion is large, or when carrying out a repeat operation, it is easy to destroy bump 1a from the circumference of a semiconductor device 13.
[0081] as [showed / the bump 1 / when thickness of the stress relaxation layer 5 was made thin about the

circumference approach of a semiconductor device 13, and it became possible to control the configuration of the corresponding bump 1 of a part and connected with the circuit board 14 / as it was in this example, / drawing 25 -- longwise -- it is set to bump 1aa. such -- longwise -- in bump 1aa, since the volume itself is the same as that of the other bumps 1, the contact angle of a bump 1 and the bump pad 3 and the contact angle of a bump 1 and the pad on the circuit board 14 become large. That is, it is set to alpha1>alpha2 and beta1>beta2 in drawing 25 .
[0082] The stress concentration to the connection of a bump and Bud will be eased because a contact angle becomes large. Thus, the connection dependability of a semiconductor device 13 and the circuit board 14 can be raised by making thickness of the stress relaxation layer 5 thinner about the bump pad 3 formation part of the periphery of a semiconductor device 13 than other parts, and making a bump's 1 configuration longwise. In addition, the cross-section configuration of the stress relaxation layer 5 can be designed within limits which do not have trouble at the time of connection of as opposed to the circuit board 14 of a semiconductor device 13 in a bump's 1 height, and can consider various things.
[0083] The magnitude of delta is determined in consideration of the bump height variation allowed value at the time of the functional test of the stress relaxation characteristic required of aa and the longwise bump 1(2) semiconductor device 13 which are located in the (1) outermost periphery, the bump height variation allowed value at the time of the connection to the circuit board 14 of the (3) semiconductor device 13, etc. If it describes more concretely, the above-mentioned stress relaxation characteristic can be found from the elastic modulus of the stress relaxation layer 5, and the size of a semiconductor device 13. On the other hand, about the variation at the time of a functional test and connection, after also taking into consideration deformation of a solder ball and the stress relaxation layer 5, those allowed values are calculated. For example, if a functional test pushes an inspection fixture from a bump top face and is made to deform the stress relaxation layer 5, it can carry out a functional test in the condition that bump height variation does not exist substantially. Even if it performs such actuation, since the modulus of elasticity is fairly low compared with a solder bump ingredient, rather than deformation of a solder bump, deformation of the stress relaxation layer 5 gives priority to the stress relaxation layer 5, it happens, and a blemish is not attached to a solder bump. So, even if the value of delta demanded from a stress relaxation characteristic becomes larger than the bump height variation demanded with functional test equipment, if it is the range which can respond according to deformation of the stress relaxation layer 5, it will not interfere. Moreover, since a stress relaxation ingredient is an elastic body, and a configuration is restored after inspection termination, there is no special problem also at the time of connection with a substrate. A consideration of this will determine (3) to the above (1) and delta as a matter of fact. As mentioned above, since, as for a stress relaxation characteristic, 35 thru/or a good result are obtained for the thickness of the stress relaxation layer 5 by 150 micrometers, it becomes delta=150-35=115 micrometer from a stress relaxation characteristic. Moreover, the value of delta= 115 micrometers is almost equal to the upper limit to the circuit board 14 permitted in the case of connection. Therefore, the value of delta turns into a upper limit, when 115 micrometers is many.
[0084] Moreover, detailed-ization of a semiconductor device progresses, and on the relation of wiring of a semiconductor device, the structure of this example can be adapted, also when a bump must be formed in the ramp of a stress relaxation layer. In addition, although the thickness of the stress relaxation layer 5 is controlled by above-mentioned drawing 24 in order to distinguish between height by outermost periphery bump 1a and bump 1b of the one inside, there is also an approach by the structural adjustment of a protective layer 8 as the other control approaches. For example, as shown in drawing 40 , the organic layer of a protective coat 8 is not formed directly under outermost periphery bump 1a, or it limits for forming very thinly, and inside bump 1b, there is the approach of forming the organic layer of a protective coat 8 more thickly. A problem does not have attaining the desired height difference delta in any way by adjusting suitably the thickness of the stress relaxation layer 5, and the organic bed depth of a protective layer 8, and controlling them if needed,, either.
[0085] Moreover, since external force tends to join the bump located in the outermost periphery of a semiconductor device and a crack etc. may be made to solder, some may be used as a buffer member among the bumps located in the outermost periphery. In this case, as for the bump who uses it as a buffer member, it is desirable to consider as an unnecessary thing, when the semiconductor device which is not electrically connected with the aluminum pad 7 operates electrically. A period until fracture occurs by the bump of required others when a semiconductor device operates electrically by this is extensible. In addition, about some bumps who

consider as a buffer member, enlarging the diameter of a bump can also extend the period to bump fracture further. In addition, in this example, in order to enlarge the suitable diameter of a bump, which approach of well-known common use may be used, but when one suitable approach is illustrated especially, the volume of solder itself is enlarging a bump land (pad), making it the same as that of other bumps. While the diameter of connection becomes large by enlarging a pad, since it is the same as others, bump height becomes low, as the result, the contact angle of a bump and a pad becomes large and the volume of solder can avoid the stress concentration to the point of contact of a pad with a bump, when it connects with the circuit board 14. Since the absolute value of crack die length when the diameter of a bump increased, until it results in fracture itself is large while crack progress within solder becomes slow, when stress concentration was lost, a bump contributes to the period extension to a stage greatly.

[0086] Moreover, if it thinks from a viewpoint of making easy the design of the wiring drawer of the circuit board which connects a semiconductor device It is desirable to arrange a power source or a grand line near the center of a semiconductor device. As the result As for the wiring 4 for rewiring which connects a bump pad with a near distance from the aluminum pad 7 and an aluminum pad as shown in drawing 26 (a) and (b), it is [the wiring 4 for the maximum wiring which connects a far bump pad as a signal line] desirable to use as a power source or a grand line. In this case, the bump with a near distance from an aluminum pad may be located in the ramp of the stress relaxation layer 5. Moreover, a power source or a grand line may be made to make wiring width of face larger than a signal line.

[0087] Other examples of a semiconductor device are shown in drawing 27 . At this example, the stress relaxation layer 5 is formed, where the semiconductor device 13 of the next door on the wafer 9 with which the semi-conductor was formed is straddled. The device on a design is made so that, as for the aluminum pad 7, the bump pad 3, and the wiring 4 for rewiring that connects these, the wiring 4 for rewiring may not cross the boundary of a semiconductor device 13 and the next semiconductor device 13. Although the production process is fundamentally [as what was already explained] the same, there is a difference after the seventh process.

[0088] In case a semiconductor wafer is cut, cutting of the stress relaxation layer 5 is also needed, but since the stress relaxation layer 5 is a low spring material, it is difficult for bundling up with the wafer 9 with which the semi-conductor with which most consists of silicon and reinforcement differs was formed, and cutting. For this reason, after performing cutting to the stress relaxation layer 5 first, the dicing of the wafer 9 with which the semi-conductor was formed is carried out. Hereafter, it explains using drawing 28 .

[0089] First, only the stress relaxation layer 5 is cut at the seventh amelioration process. It is good to use the rotary knife suitable for cutting of a low elastic resin ingredient as a cutting process. In addition, carbon dioxide gas laser, sandblasting, etc. can be used.

[0090] In the eighth amelioration process, a solder resist is applied to the whole surface as a surface protective coat 6. Printing and curtain coating using the mask of the shape of a mesh besides a spin coat method as the method of application are sufficient. Also in order to apply a solder resist, the wall surface of the cutting section of the stress relaxation layer 5 in the seventh amelioration process is not perpendicular, and it is desirable to mak it become the shape of reverse Ha's character. By performing this coating after cutting of the stress relaxation layer in the seventh amelioration process, the stress relaxation layer 5 can become the factor which exfoliates from the front face of a wafer 9 in which the semi-conductor was formed, or invasion of foreign matters, such as ion which causes the performance degradation of a semi-conductor, can be mitigated, and the device which secured endurance etc. can be offered.

[0091] In the ninth amelioration process, the pattern of the surface protective coat 6 is formed by performing sensitization development. Thereby, only the bump pad 3, the cutting section 24, and its circumference are exposed from the surface protective coat 6. Moreover, gold is formed on the bump pad 3 by giving non-electrolyzed gilding by using the surface protective coat 6 as a mask. In addition, although considered only as gilding in the example, you may give, before plating the plating of palladium or platinum with gold, and even if performs tinning after gilding termination, there is no special problem.

[0092] In the tenth amelioration process, the wafer 9 with which the semi-conductor was formed of dicing is divided into a semiconductor device 13. In addition, generally dicing is performed using a rotary knife.

[0093] Manufacture of the semiconductor device 13 which includes the process which cuts the stress relaxation layer 5 according to the above process is attained.

[0094] According to this example, even when the dimension of a semiconductor device 13 is small, it becomes possible to form the stress relaxation layer 5 satisfactory. In specifically forming the stress relaxation layer 5 ranging over two adjacent semiconductor devices Even if a dimension becomes half mostly, it is not necessary tc change the membrane formation technique of the stress relaxation layer 5. Even if it changes the magnitude of a semiconductor device by adjusting the width of face of the cutting section 24 which is cutting at the time of separating the configuration of a semiconductor device, a dimension, and the semiconductor device 13 of each other, and a configuration, manufacturing using the same printing mask may even become possible. Moreover, since the wiring 4 for rewiring has connected the aluminum pad 7 and the bump pad 3 through the ramp of the stress relaxation layer 5 like the first example, stress raisers do not exist in the wiring 4 for rewiring, either, but the flip chip bonding of it which does not need under-filling becomes possible.
[0095] In addition, especially the structure concerning this example can be adapted for the semiconductor device with which the pad was arranged by the pin center,large part of a semiconductor device, for example, DRAM etc

[0096] Moreover, although the stress relaxation layer 5 over two adjacent semiconductor devices 13 was cut in drawing in this example, as long as the slope section for the wiring 4 for rewiring to result [from the aluminum pad 7] in the bump pad 3 exists, it is also possible to adopt the structure where the stress relaxation layer 5 connected about the semiconductor device 13 of at least 2 more than, for example, four semiconductor devices which adjoin each other mutually, is cut. The connected stress relaxation layer 5 is formed and you may make it cut it about two trains which adjoin each other with a natural thing. In this case, since it becomes the process which can permit a location gap of the direction of a train, it is more applicable also to micro processing.
[0097] In each example, as shown, for example in drawing 2 or drawing 27 , it is good for the corner of the stress relaxation layer 5 to give a radius of circle. When it does not give a radius of circle, in case the stress relaxation layer 5 is printed using a paste-like polyimide ingredient, it sometimes gazes at the defect who involves in air bubbles. Moreover, the stress relaxation layer 5 becomes easy to exfoliate from a corner. If air bubbles remain in the stress relaxation layer 5, when a semiconductor device 13 is heated, air bubbles will explode and the fault of the wiring 4 for rewiring being disconnected will arise. For this reason, as for the corner of the pattern opening 1 of the metal mask for printing used for formation of the stress relaxation layer 5, rounding off is desirable.
[0098] In addition, using the metal mask for printing, or a dispenser, printing spreading of the stress relaxation layer 5 in each example can be carried out, and it can be formed.
[0099] Moreover, it can form approaches, such as sticking the resin sheet of not only the printing approach but a **********, air or blasting and the ink jet method using inactive gas, un-hardening, or a semi-hardening condition, or by combining these approaches suitably. When forming a stress relaxation layer by the printing approach, and the inclination of a printing section edge prints an insulating material and a printing mask is removed, in a heat hardening process, a flow of an insulating layer takes place at the end, and the ramp of an edge is formed. It is possible to create the edge which has a stress relaxation layer and a specific inclination per wafer by this approach by package. On the other hand, when forming a stress relaxation layer by the stamping, since the insulating material for stress relaxation is applied to the mold for ********** and the configuration of a stress relaxation layer is imprinted on a wafer, selection of the insulating material which form status change-ization of the edge at the time of insulating material hardening does not produce is attained. In this case, there is the description that the configuration of an edge tends to become fixed compared with a printing method. Furthermore, by the method which sprays an insulating material using gas etc., if those with a degree of freedom and nozzle dimensions are suitably chosen as the configuration at the time of the stress relaxation stratification ir order not to use a printing mask or ********** metal mold, in a printing mask or ********** metal mold, formation of the stress relaxation layer which is hard to form will be attained. Moreover, compared with a printing method or a ********** method, the thickness of a stress relaxation layer can be adjusted by adjustment of the amount of blasting, and the range of thickness adjustment also becomes large. By the method which sticks the resin sheet which is not hardened [semi-hardening or], in order to attain formation of the stress relaxation layer of a thick film and to use insulating sheet-like resin beforehand, there is the description of excelling in the surface smoothness of a stress relaxation layer front face. It becomes possible about these approaches to obtain desired stress relaxation layer thickness and an edge inclination a single or by combining suitably.

[0100] Next, other examples of a semiconductor device are shown. the cross-section schematic diagram showing the condition of having carried drawing 29 in the substrate for changing the projection electrode of a semiconductor device, and drawing 30 are the cross-section schematic diagrams showing the condition of having closed the clearance between a semiconductor device 13 and the substrate in which this is carried by resin 118 further -- it comes out.
[0101] The letter electrode 1 of a projection formed in the semiconductor device 13 is carried through a ********-strike or flux on the electrode 120 with which it corresponds on a substrate, melting of said letter electrode of a projection is carried out at a reflow furnace etc., and connection of a substrate 115 and a semiconductor device 13 is made. The substrate carrying a semiconductor device has the letter electrode 121 of a projection if needed [an electrode 120 and if needed] for carrying in the substrate used for various electronic equipment at the rear face of a semiconductor device loading side.
[0102] In case a semiconductor device 13 is carried in the substrate used for various electronic equipment, it is necessary to carry out heating melting of the letter electrode 121 of a projection prepared on the substrate 115. In order to raise further these mounting processes and the dependability in various trials, especially the dependability results over a drop impact test, between a semiconductor device 13 and substrates 115 is reinforced by resin 118.
[0103] The resin 118 filled up with between a semiconductor device 13 and a substrate 115 The liquefied epoxy resin used for the general semi-conductor closures, phenol resin, In order polyimide resin, silicone resin, etc. are usable and to adjust the coefficient of thermal expansion and elastic modulus of closure resin A silica, Or two or more kinds are blended. the particle which consists of inorganic materials, such as an alumina and boron nitride, - one kind -- Moreover, it is possible to blend the hardening accelerator for promoting the hardening reaction of the flame retarder for making the coupling agent and coloring agent which consist of resin, such as silicone and thermoplastics, alkoxysilane, titanate, etc. if needed, and fire retardancy give, or a fire-resistant assistant resin layer etc.
[0104] In this example, even if it is the case where the pitch of the letter electrode of a projection on a semiconductor device differs from the pitch of the electrode of the substrate used for various electronic equipment, it becomes possible by minding a predetermined substrate to connect with various electronic equipment.
[0105] In addition, also when you mount in the circuit board used for general electronic equipment like mounting to the substrate used as a semiconductor device, suppose that it is the same.
[0106]
[Effect of the Invention] According to this invention, the semiconductor device which makes possible unnecessary flip chip bonding of under-filling is realized.

[Translation done.]

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the structure and the manufacture approach of a semiconductor device aiming at flip chip bonding.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Many of semiconductor devices have a laminated structure, and the insulating laye is arranged between each class in many cases. Opening is prepared in this insulating layer, it lets that opening pass, and wiring which connects a lower layer terminal and the upper terminal is formed.
[0003] The following approaches are adopted as the insulating stratification approach. That is, a photosensitive insulating material is applied with a spin coat method on a semiconductor device, and opening of an insulating layer is formed by carrying out exposure and development. Moreover, metal wiring which connects a lower laye terminal and the upper terminal applies the second photosensitive ingredient to the insulating-layer upper layer, forms a mask by performing exposure and development to this, and forms metal wiring which connects the terminal and the upper layer of the insulating-layer lower layer in using together processes, such as this, plating, spatter, CVD, and vacuum evaporationo. This is removed after becoming unnecessary [the photosensitive insulating material used as a mask].
[0004] Formation of wiring which connects the terminal in the lower layer of an insulating layer and the upper layer according to the above process is attained. The fragmentary sectional view of the semiconductor device formed of such a process is shown in drawing 31 . In this drawing, the aluminum pad 7 serves as a terminal of insulating-layer 12 lower layer, and the bump pad 3 serves as a terminal of the insulating-layer upper layer. And as for the insulating layer 12 formed on the wafer 9 with which the semi-conductor was formed, opening is prepared on the aluminum pad 7. Moreover, the metal wiring 11 is formed from the aluminum pad 7 even to the bump pad 3 of the upper layer of an insulating layer 12. The bump 10 is formed in the bump pad 3. In addition, i is called rewiring to form wiring from the aluminum pad 7 to the bump pad 3 in this way. Moreover, the thickness of the insulating layer 12 in this case is almost equivalent to the thickness of the metal wiring 11.
[0005] Flip chip bonding is in one of the gestalten which mount the semiconductor device manufactured through such a process on the circuit board like a printed wired board, and are connected. Drawing 32 is the sectional view of the semiconductor device which carried out flip chip bonding. Connection between a semiconductor device 13 and the circuit board 14 is made because the bump 10 prepared on the terminal of a semiconductor device 13 solidifies again after melting on the circuit board. The gap of a semiconductor device 13 and the circui board 14 is filled up with the resin of high rigidity. In addition, this resin is called under-filling 15 and is effectiv in reinforcing a connection. There is JP,11-111768,A as an example of the flip chip bonding which carried out under-filling.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the semiconductor device which makes possible unnecessary flip chip bonding of under-filling is realized.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, there are the following problems in the above-mentioned conventional technique.

[0007] Difficulty is in the supply approach of the resin to the gap of a semiconductor device and the circuit boarc in the first place. That is, the method of using capillarity is taken as an approach a clearance supplies resin to the gap which is generally 0.3mm or less. However, since the resin ingredient for under-filling is hyperviscous liquefied resin, it requires the time amount embedded in a clearance, and has the problem of an air ball tending tc remain.

[0008] Difficulty is [second] in removal of a semiconductor device. That is, in order that the hardened under-filling ingredient may remain on the circuit board even after removing even if it removes this semiconductor device from on the circuit board when the semiconductor device linked to the circuit board is a defective, the problem that playback of the circuit board is difficult exists.

[0009] Also in order to solve the first and the second trouble, it is desirable to connect a semiconductor device to the circuit board, without carrying out under-filling. However, under-filling is carried out in order to prevent destruction of the connection resulting from distortion produced in the connection by generation of heat at the time of using the completed electric product etc., and in not carrying out, the problem that the connection life of semiconductor device will become extremely short arises. Moreover, when forming a solder bump in the semiconductor device which makes possible unnecessary flip chip bonding of under-filling, by collapse of the impurity contained in the solder bump, alpha rays occur and malfunction of the transistor section may be caused.

[0010] The purpose of this invention is to realize the semiconductor device which makes possible unnecessary flip chip bonding of under-filling.

MEANS

[Means for Solving the Problem] This invention is constituted as a claim, in order to attain the above-mentioned purpose. Thus, the above-mentioned purpose is attained by forming wiring on a desired insulating layer (thick-film insulating layer). For example, destruction of a connection can be prevented by using the ingredient of low elasticity for the insulating layer of a semiconductor device, and forming an insulating layer with a thickness of 35 microns or more. Moreover, it becomes possible to reduce sharply the stress produced in a connection in the insulating layer of low elasticity existing. By this, the connection life of a semiconductor device improves sharply. Moreover, not only easing the stress produced to a wafer etc. but unnecessary alpha rays can be intercepted by making an insulating layer into predetermined thickness. [0012] Moreover, when adopting the insulating layer of the thick film of about 35 micrometers or more, it is hard to apply the conventional wiring formation approach. Since the ingredient for insulating stratification is hyperviscosity, it will become an insulating layer containing air bubbles, and will stop that is, achieving the function as an insulating layer in a spin coat method, when carrying out thick-film formation of the insulating layer. Even if it develops the new thick-film formation approach apart from this, since the permeability of light falls, in 35-micrometer thickness, it is difficult to carry out pattern formation of the opening of an insulating layer etc. with high precision in exposure development. ****** this problem is solvable -- the side attachment wall of opening of an insulating layer -- ** beyond about 80 degrees and it -- since that height serves as a sharply larger value than wiring thickness perpendicularly, metal wiring becomes that it is hard to be formed in a side attachment wall. Moreover, since the flection of metal wiring is formed in the boundary section of a side attachment wall and the upper layer even when it is able to form even if, it is easy to concentrate stress on this location, and, for this reason, a crack tends to progress. For this reason, the connection life at the time of circuit board connection will become short.
[0013] Since the flection of metal wiring which a thick-film insulating layer is formed, and formation of wiring on an insulating layer is attained with the conventional method of construction by making the configuration of insulating layer opening into a gently-sloping slant face, and stress concentrates there by carrying out mask printing of the insulating material containing a minute particle does not exist, either, it is hard to produce an open circuit of wiring. Moreover, the property of a thick-film insulating layer is changed in the thickness direction. For example, near is carried out to the property of a substrate of carrying the property of a thick-film insulating layer by the semiconductor device side, and carrying these in a semiconductor device by the near and electrode side. As stress does not concentrate on wiring formed on the thick-film insulating layer by this, dependability can be raised further. That is, an open circuit can be controlled further. In addition, on these specifications, this thick-film insulating layer is indicated to be a stress relaxation layer.
[0014]
[Embodiment of the Invention] Hereafter, it explains, using drawing together about one example of this invention. In addition, in all drawings, in order that the same sign may have omitted the explanation which overlaps since the same part is shown and may give explanation easy, it has changed the proportion of each part with the actual condition.
[0015] First, the structure of the semiconductor device by this example is explained. Below, although it is collectively manufactured by many per wafer, in order to give explanation easy, a semiconductor device takes out the part and is explained. The fragmentary sectional view of the semiconductor device 13 of this example is shown in drawing 1 .

[0016] The wafer 9 with which the semiconductor circuit was formed is a wafer which ended the last process as used in the field of a semi-conductor production process, and is a thing before division cutting at many semiconductor devices 13. The connection terminal 7 for the exteriors, for example, an aluminum pad, is formed in each semiconductor device 13. In the semiconductor device 13 of a conventional type, when storing in semiconductor packages, such as QFP (Quad Flat Package), this aluminum pad 7 connects a golden wire etc., an it is used in order to realize a flow with the external terminal of a semiconductor package. The front face of a semiconductor device 13 in which the semiconductor circuit was formed is covered with the protective coat 8 except for the cutting section 24 at the time of cutting the wafer 9 with which the aluminum pad 7 top and many semi-conductors were formed to the chip-like semiconductor device 13, and its circumference. The insulating resin which becomes this protective coat 8 from the insulating resin independent or the organic material which consists of thickness 1 thru/or an about 10-micrometer inorganic material is used together. The bipolar membran which carried out the laminating of the organic compound insulator which becomes the upper part of independence or said inorganic insulator layer from an organic material about the insulator layer which consists of thickness 1 thru/or an about 10-micrometer inorganic material is used for this protective coat 8. When using this bipolar membrane, as for this organic film, it is desirable to use a photopolymer ingredient. When a photosensitive ingredient suitable as organic film of a protective coat 8 is illustrated by this example, there are photosensitive polyimide, photosensitive benz-cyclo-butene, photosensitive poly benzoxazole, etc. In this example, the inorganic material, the organic materials, or such bipolar membrane of well-known common use can be used not only as this but as a protective coat. For example, SiN, SiO2, etc. can be used as inorganic film. Moreover, although it does not matter even if it is formed so that the whole surface may be covered mostly, of course, as shown in drawing 33 , even if this organic film is formed only in the field of the inorganic film which becomes near the aluminum pad 7, it is not cared about, and as shown in drawing 34 , it may be formed only in two or more places of the arbitration of an inorganic film front face. Thus, by limiting the field of the organic film, the curvature of the wafer 9 by the internal stress of a protective coat 8 is reduced, and it becomes advantageous in respect of the handling in a production process, focusing at the time of exposure, etc. In additior in this example, the field near the aluminum pad 7 has pointed out the field from the edge of the aluminum pad 7 to 1mm of maximum distances. In addition, in drawing 33 and drawing 34 , although the organic film around the aluminum pad 7 is formed in the continuation field, it may be formed in the field which became independent for each aluminum pad of every, respectively. Specifically, it becomes a field like drawing 35 . In view of the patter precision of the photopolymer used for this organic film, membranous internal stress, and the component property of this semiconductor device, it determines whether which gestalt of drawing 35 is used from drawing 33 . If an example of the component property said here is given, it has pointed out changing the level of the energy barrier in each active cell inside a component (transistor) according to the stress operation to this semiconductor device.

[0017] On the protective coat 8, thickness 35 thru/or the 150-micrometer stress relaxation layer 5 are formed alternatively. Although the thickness of a stress relaxation layer is dependent on the size of a semiconductor device, the elastic modulus of a stress relaxation layer, semiconductor device thickness, etc. and cannot generally be ******(ed) The semiconductor device thickness generally used is about 150 thru/or 750 micrometers. The place which conducted the stress simulation experiment with the bimetal model which consists of a semiconductor device and a stress relaxation layer formed in the front face, Since, as for necessary stress relaxation layer membrane thickness, it turned out that 10 thru/or 200 micrometers are 35 thru/or 150 micrometers desirable still more preferably, this example was formed in this thickness range. About 1/of this is equivalent to about 20 to 1/5 thickness to the thickness of a semiconductor device. If thickness becomes smaller than 35 micrometers, desired stress relaxation cannot be obtained, and if thickness becomes thick exceeding 150 micrometers, the curvature of a wafer will occur for the internal stress which stress relaxation layer 5 self has, and it becomes easy to generate the handling fault in focus gap, a wiring formation process, etc. in an exposure process etc., and there is a problem that productivity falls. The stress relaxation layer 5 is formed with the resin ingredient which has the elastic modulus of 0.1GPa(s) to 10GPa(s) in an elastic modulus sharply smaller than a semiconductor wafer 9, for example, a room temperature. If it is the stress relaxation layer which has the elastic modulus of this range, a reliable semiconductor device can be offered. That is, in the case of the stress relaxation layer of the elastic modulus which is less than 0.1GPa, in case it becomes difficult to support the weight of the

semiconductor device itself and it uses it as a semiconductor device, it is easy to produce the problem that a property is not stabilized. On the other hand, when the stress relaxation layer of the elastic modulus exceeding 10GPa is used, there is even a danger that the curvature of a wafer will occur for the internal stress which stress relaxation layer 5 self has, will become easy to generate the handling fault in focus gap, a wiring formation process, etc. in an exposure process etc., and the fault that a wafer breaks further will occur. The edge section of the stress relaxation layer 5 has the inclination, and the average gradient is 5 thru/or about 30%. In the case of the tilt angle which is less than 5%, an inclination becomes long too much and desired thickness is not obtained. For example, in order to consider as the thickness of 100 micrometers with the tilt angle of 3% of average gradients, desired thickness will be obtained, if about 7 millimeters cannot be found when the horizontal distance of 3-millimeter ** is needed and the edge section on either side is united. On the other hand, although it is satisfactory in respect of horizontal distance when a tilt angle is 30% **, the danger that step coverage conversely sufficient in the case of wiring formation will not be obtained is high. Especially plating resist is attached, there is no process margin in the process of the surroundings, exposure, and development, and special skill or a special technique is needed. When a tilt angle is still larger, the so-called stress concentration effectiveness may act, stress may concentrate on the edge section, the inclination an open circuit of the wiring 4 for rewiring becomes easy to generate in the edge section as the result may appear, and a device special to wiring structure may be needed. Since it is 50-micrometer thickness from the edge of the stress relaxation layer 5 with the horizontal distance of 500 micrometers in the case of drawing 1 , an average gradient is 10%. The wiring 4 for rewiring is formed with conductors, such as copper, and has connected the aluminum pad 7 and the letter electrode 3 of a projection of stress relaxation layer 5 front face, for example, a bump pad. Moreover, the bump pad 3 top may form the gilding 2 for preventing oxidation of the bump pad 3. The front face of a semiconductor device 13 is covered by the surface protective coat 6 except for the cutting section 24 at the time of cutting the wafer 9 with which the bump pad 3 and many semi-conductors were formed to each semiconductor device 13.

[0018] Since it is closing by covering completely a protective coat 8 and the stress relaxation layer 5 by the surface protective coat 6, it prevents that a protective coat 8 and the stress relaxation layer 5 exfoliate from the front face of a wafer 9 in which the semiconductor device was formed, and invasion of foreign matters, such as ion which causes the performance degradation of a semi-conductor, can also be mitigated. Moreover, since the protective coat 8, the stress relaxation layer 5, and the surface protective coat 6 are all retreating from the cutting section 24, in case they carry out cutting separation of the semiconductor device 13, they do not receive damage.

[0019] The various resin ingredients which have an electrical insulating characteristic as a surface protective coat 6 can be used. Although it is desirable that it is a photosensitive ingredient since it is necessary to form a pattern, membranes may be formed by printing, for example using the ingredient corresponding to high precision printing of an ink jet etc. In addition, after carrying out solid formation of the insulator layer by the cheap methods of application, such as a curtain coat, a photolithography process may be used, and patterning of the etching resist may be formed and carried out, and membranes may be formed through the process of etching processing and resist exfoliation for the above-mentioned insulator layer using this resist pattern. Although various ingredients are usable in this example as such an ingredient, if some are illustrated, denaturation triazole resin, denaturation melamine resin, polyimide resin, etc. will be suitably used as (1) photosensitivity ingredient as polyamidoimide resin, polyimide resin, and a charge of (3) solid membrane formation material as an acrylic denaturation photosensitivity epoxy resin, photosensitive polyimide resin, and a (2) ink-jet printing ingredient. If it illustrates still more concretely about a photosensitive ingredient, the photosensitive polyimide used for surface covering of a solder resist or a flexible printed circuit board used suitably will be suitably used as a surface protective coat 6 by the printed circuit board production process as a cheap photopolymer ingredient. On the other hand, as a charge of solid membrane formation material, photograph NISU TM of Toray Industries, Inc. etc. is suitable, for example. In addition, the solder resist was used in this example. The bump 1 is formed on the bump pad 3. As for this bump 1, forming with a solder ingredient is common. A bump 1 becomes an external connection terminal here.

[0020] The top view which omitted the bump 1 who originally exists the condition that the semiconductor device 13 shown in drawing 2 by drawing 1 is continuously formed on the wafer showed. The part shown by hatching in drawing 2 is the solder resist which is the surface protective coat 6. Moreover, it is formed in the condition that the stress relaxation layer 5 is formed in the shape of [which rounded off the angle] a rectangle, and gets down,

and the cutting section 24 which is cutting at the time of separating each semiconductor device 13 exists betweer each semiconductor device 13. cut -- it is desirable to be located in 10 thru/or 100 micrometers from the edge of ** 6, for example, a surface protective coat. If there is an inclination which becomes easy to induce a chipping and it becomes conversely longer than 100 micrometers in case each semiconductor device will be separated, if shorter than 10 micrometers, an effective area usable as a semiconductor device will decrease. Therefore, it is desirable to locate spacing with the surface protective layer 6 in 10 thru/or 100 micrometers by this example as cut and carry out for the improvement in the yield of a semiconductor device 13. In addition, although not illustrated by the lower layer of the end of the wiring 4 for rewiring, the aluminum pad 7 exists in it.

[0021] According to this semiconductor device structure, since the stress relaxation layer 5 exists between the wiring 4 for rewiring, and a wafer 9, a semiconductor device 13 is connected on the circuit board 14, and in case it operates, it becomes possible to distribute distortion by the heat which a bump 1 receives. For this reason, it becomes possible to prolong a connection life, without carrying out under-filling 15, even if it carries this semiconductor device 13 in the circuit board 14. Moreover, since the stress relaxation layer 5 has the gently-sloping ramp, the wiring flection which turns into stress raisers in the middle of the wiring 4 for rewiring does not exist.

[0022] An example of the production process of the semiconductor device 13 in this example is explained using drawing. By drawing 3 , drawing 4 explains the sixth process from the fourth process, and drawing 5 explains th ninth process for from the first process to the third process from the seventh process. In addition, also in which drawing, cross-section structure of the semiconductor device 13 in this example is used as the sectional view which took out the part so that intelligibly.

[0023] The first process: Manufacture at the same process as the conventional semiconductor device 13 about th wafer 9 with which the semi-conductor whose aluminum pad 7 for external connection is formation ending was formed. Although the quality of the material of the pad for external connection was aluminum in the semiconductor device used by this example, an external connection pad may be copper. It is because wirebondin is not used as external connection, so it is not necessary to take into consideration the problem of the bonding nature which is easy to produce when an external connection pad is copper in this example. Since the electric resistance of wiring can be reduced if an external connection pad is copper, it is desirable also from a viewpoint of the improvement in an electrical property of a semiconductor device.

[0024] The second process: Form a protective coat 8 if needed. A protective coat 8 may already be formed in the so-called last process in a semi-conductor production process using an inorganic material, and also on an inorganic material, an organic material may be used for it and it may form it in piles. In this example, on the silicon dioxide formed of the silicon nitride formed by the insulator layer which consists of an inorganic material formed at the so-called last process in a semi-conductor process, for example, a CVD method etc., a tetra-ethoxy silane, etc., or the insulator layer which consists of those bipolar membrane, the photosensitive polyimide which is an organic material is applied and the protective coat 8 with a thickness of about 6 micrometers is formed by exposing, developing and hardening this. Thereby, a protective coat 8 is formed on the wafer 9 with which the semi-conductor was formed. Although thickness of a protective coat 8 was made into 6 micrometers in this example, necessary thickness changes with classes of the semiconductor device concerned, and the range becomes 1 thru/or about 10 micrometers. In addition, although it does not matter even if it is formed so that the whole surface may be covered mostly, of course, as shown in drawing 33 - drawing 35 , even if this organic film is formed only in the field of the inorganic film which becomes near the aluminum pad 7, it is not cared about as shown in drawing 13 . In the case of the insulator layer which consists only of an inorganic material, the range of thickness becomes 3 micrometers or less. Moreover, poly benzoxazole, poly benz-cyclo-butene, the poly quinoline, poly FOSUFAZEN, etc. can be used besides the photosensitive polyimide used in this application example.

[0025] The third process: Carry out printing spreading of the paste-like polyimide ingredient in the formation schedule part of the stress relaxation layer 5, and make it harden by heating this after that. Thereby, the stress relaxation layer 5 is formed on a protective coat 8.

[0026] The fourth process: Use the reverse pattern 17 of wiring and form a photoresist, after forming the electric supply film 16 for using for electroplating by approaches, such as a spatter.

[0027] The fifth process: Perform electroplating using this electric supply film 16 and the reverse pattern 17 of

wiring, and perform formation of the wiring 4 for rewiring, and the bump pad 3. Moreover, wiring 4 for rewiring is made into multilayer structure by repeating electroplating if needed.
[0028] The sixth process: Etching processing removes the reverse pattern 17 of wiring which consists of a photoresist, and the electric supply film 16 of electroplating.
[0029] The seventh process: Form the surface protective coat 6 using a solder resist. And non-electrolyzed gilding 2 is performed on the maximum front face of the bump pad 3 using this pattern.
[0030] The eighth process: On the bump pad 3, connect a solder ball to the bump pad 3 by carrying and heating a solder ball with flux, and form a bump 1.
[0031] The ninth process: A wafer dicing technique cuts the wafer 9 with which the semi-conductor was formed to a semiconductor device 13.
[0032] Below, it attaches by the eighth process from the third above-mentioned process, and explains to a detail.
[0033] First, the third process is explained. The mask used for printing has the usable thing of the same structure as the mask for printing used by soldering paste printing to a printed wired board etc. For example, as shown in drawing 6 , the metal mask of the gestalt which stuck the stencil 25 made from a nickel alloy on the frame 27 through the resin sheet 26 can be used. Since a paste is damp and about 50 micrometers of pattern openings 28 o the mask for printing spread after printing, you may make it manufacture them the part and smallness which expected it. As shown in drawing 7 , it is that paste printing sticks the mask for printing, and the pattern of the wafer 9 with which the semi-conductor was formed where alignment is carried out, and a squeegee moves in the condition in a stencil 25 top, and is filled up with the pattern opening 28, and it is raising the mask for printing relatively after that to the wafer 9 with which the semi-conductor's was formed, and the so-called contact printing which prints is performed. In addition, adhesion of the wafer said here and the mask for printing does not necessarily mean completely losing a clearance among both. Since the protective coat 8 is already partially formed on the wafer, it is because it is difficult practically to stick a printing mask without a clearance on this. A this example, it printed on printing conditions from which the clearance between a wafer and the mask for printing becomes 0-100 micrometers. In addition, the whole squeegee side of the mask for printing is coated with the first squeegee with a paste, the pattern opening 28 of the mask for printing is filled up with the second squeegee after that, and an excessive paste is removed. Then, there is also the printing approach of raising the mask for printing relatively to the wafer 9 with which the semi-conductor was formed. You may make it go up, although you may make it go up perpendicularly as shown in drawing 8 in case a printing mask is relatively raised to a wafer 9, moving so that it may have a tilt angle relatively. By giving a tilt angle, a version detached building angle in case a printing mask separates from a wafer tends to become homogeneity in a wafer side. Moreover, the printing mask will separate from one edge of a wafer toward the other end, at the moment of the last of a version detached building when a version omission tends to become unstable, will be performed in a field without a semiconductor device. and becomes advantageous also in respect of the improvement in the yield Furthermore, when performing continuous printing to two or more sheet wafer using the same printing machine, it is good to insert the process which wipes the background of the mask version with proper timing. For example in this example, when ten-sheet continuation printing was carried out, the background of the mask version was cleaned once, and printing of the 11th sheet was performed after an appropriate time. As for the timing of cleaning of a mask background, a count, and its approach, accommodation is needed suitably with the viscosity and solid content concentration of a paste ingredient, the amount of fillers, etc.
[0034] A paste hardens by heating gradually the wafer 9 with which the semi-conductor with which printing spreading of the paste was carried out succeedingly was formed using a hot plate or a heating furnace, and formation of the stress relaxation layer 5 is completed.
[0035] The ingredient for formation of the stress relaxation layer 5 currently used here is paste-like polyimide, and can be hardened by heating, after printing spreading is carried out on a protective coat 8. Moreover, the polyimide of the shape of this paste consists of a minute particle of the polyimide of a large number distributed the precursor of polyimide, a solvent, and in it. As a particle, it is specifically mean particle diameter 1 thru/or 2 micrometers, and the minute particle which has the particle size distribution from which a maximum grain size becomes about 10 micrometers was used. Since the precursor of the polyimide used for this example will serve a the same ingredient as the minute particle of polyimide if it is hardened, when paste-like polyimide hardens, the uniform stress relaxation layer 5 which consists of one kind of ingredient will be formed. Although polyimide

was used as a stress relaxation stratification ingredient in this example, it is also possible in this example to use amide imide resin, ester imide resin, ether imide resin, silicone resin, acrylic resin, polyester resin, the resin that denaturalized these in addition to polyimide. When using resin other than polyimide, it is desirable to give conversion to a resin presentation so that processing which gives compatibility to the above-mentioned polyimid minute particle front face may be performed or compatibility with the above-mentioned polyimide minute particle may be improved. In the resin which has imide association among the resin which carried out [above-mentioned] listing, for example, polyimide, amide imide, ester imide, and ether imide, it excels in a heat mechanical property, for example, the reinforcement in an elevated temperature etc., thanks to the firm frame by imide association, and ****** of the plating electric supply film formation approach for wiring spreads as the result. For example, the plating electric supply film formation approach accompanied by high temperature processing, such as a spatter, can be chosen. When it is resin with the part condensed in association other than imide association, such as silicone resin, acrylic resin, polyester resin, amide imide, ester imide, and ether imide, although a heat mechanical characteristic is inferior a little, it may be advantageous in respect of workability, a resin price, etc. For example, by polyester imide resin, generally, since curing temperature is lower than polyimide, it is easy to treat. In this example, a component property, a price, a heat mechanical characteristic, etc are synthetically taken into consideration out of these resin, and these resin is used properly suitably.

[0036] Since it becomes possible to adjust the visco-elastic property of an ingredient by distributing a polyimide minute particle into paste-like polyimide, the paste excellent in printing nature can be used. Since it becomes possible to control the thixotropy property of a paste by adjusting combination of a minute particle, a printing property is improvable by combining with adjustment of viscosity. Moreover, whenever [tilt-angle / of the stress relaxation layer 5] can also be adjusted. It is desirable for the suitable thixotropy property of a paste to have the so-called thixotropy index for which it asked from the ratio of the viscosity in engine-speed 1rpm measured using the rotational viscometer and the viscosity in engine-speed 10rpm in the range of 2.0 to 3.0 in this application example. In addition, when it is the paste with which temperature dependence appears in a thixotropy index, high results will be acquired if it prints in a temperature field in which a thixotropy index becomes the range of 2.0 to 3.0.

[0037] After carrying out heat hardening of the polyimide of the shape of a printed paste, the stress relaxation layer 5 which has a cross-section configuration as shown on the wafer 9 at drawing 9 is formed. Thus, although i may swell at the place of 200 thru/or 1000 micrometers and a part may exist from the edge section of the stress relaxation layer 5 if the stress relaxation layer 5 is formed by printing, about the location of this swelling part, and the existence of existence, the presentation of paste-like polyimide is adjusted, or it is changing the various conditions in connection with printing, and becomes to some extent controllable. In addition, as various conditions in connection with printing in this case, **, such as metal mask thickness, a squeegee rate, the squeegee quality of the material, a squeegee include angle, squeegee ** (printing pressure), a version detached building rate, temperature of the wafer at the time of printing, and humidity of a printing environment, are raised Although the above-mentioned printing conditions can attain control of the height of the above-mentioned swelling part, or a configuration, there is also an approach by the structural adjustment of a protective layer 8 as the other control approaches. For example, if the formation field of the organic layer of a protective coat 8 is limited only near the pad 7 as shown in drawing 36 , it is easy to make the stress relaxation layer of the part equivalent to the organic layer upper part heaped up.

[0038] Moreover, as shown in drawing 1 , when it swells in the stress relaxation layer 5 and a part is formed positively, the deflection part of wiring 4 can be formed, it becomes the structure which is easy to absorb the stress by thermal expansion etc. by this, and an open circuit can be prevented more. It is desirable that about 25 micrometers of swelling parts which have 7 thru/or height of about 12 micrometers desirably are specifically formed at the maximum to the average thickness of the stress relaxation layer 5. If it is top-most vertices of this level, it can form enough by mask printing. For example, if a radius assumes this swelling section to be the shape of a semi-cylindrical shape which is 10 micrometers, the die length of the half-arc of the swelling section becomes (2x3.14x10 micrometers) / 2= 31.4 micrometers, and the redundancy die length of wiring will become 42.8 micrometers when it forms in every one both sides of 31.4-10=21.4 micrometer and a stress relaxation layer about the one swelling section. Thus, since the redundancy section can be prepared in wiring 4, the thermal stress which acts on wiring structure and the soldered joint section is eased, therefore reliable wiring structure can be

offered. In addition, it asks for the necessary thickness of this swelling section from the experiment and simulation which took into consideration the thickness of the stress relaxation layer 5 and an elastic modulus, the size of a semiconductor device 13, the power consumption of a semiconductor device, the physical-properties value of the circuit board 14 in which a semiconductor device is carried, etc. For example, in this example, the diagonal die length of a semiconductor device 13 is made into L millimeters. If the maximum temperature requirement which the difference of the coefficient of linear expansion of the circuit board 14 in which a semiconductor device 13 and it are carried produces by ON/OFF under the substrate loading process of 15 ppm [degree C] /and a semiconductor device 13 - actuation carries out to 200-degree Centigrade The maximum heat deformation which the wiring section receives [a substrate mounting article] by use by the real operating environment becomes 15(ppm/degree C) xL/2(mm) x200 (degree-C) =0.0015xL millimeter. Therefore, when there were about 0.002xL millimeters of redundancy die length required of the above-mentioned swelling section, I thought that it was enough. It swells from this count, the section is approximated by the shape of a semi-cylindrical shape, and it was made for the height of that swelling part to be settled in L / the range of about 2000 - L/500 millimeter to the average thickness of the stress relaxation layer 5 in this example.

[0039] When the thickness of the needed stress relaxation layer 5 is not formed by one printing and heat hardening, thickness predetermined by repeating printing and hardening of an ingredient two or more times can be obtained. For example, when a metal mask with a thickness of 65 micrometers is used using the solid content concentration 30 thru/or 40% of paste, about 50 micrometers can be obtained as thickness after hardening by two printings. Moreover, especially about the bump 1 stationed in the part which distortion tends to concentrate when a semiconductor device 13 is connected to the circuit board 14, concentration of distortion can also be eased by limiting only to the stress relaxation layer 5 of the corresponding part, and thick-film-izing thickness. for this reason -- being alike -- for example, what is necessary is just to print multiple times using a different metal mask from what used paste-like polyimide by the 1st printing to the wafer 9 top with which the semi-conductor was formed Moreover, the thickness of a stress relaxation layer can also be partially changed by adjusting the structure of a protective layer 8 as the 2nd approach. For example, as shown in drawing 37 , Bump's X field [directly under] which a strain tends to concentrate uses only the protective layer which consists of inorganic film, and uses as a protective coat the compound layer in which the organic film was formed on the inorganic film, in other fields. If a stress relaxation layer is formed on such a protective coat, a loose ramp will be formed in the parts A of a place with the protective coat of the organic film, and the stress relaxation layer which is not. Now, for the thickness of 1GPa and the organic film, in 10 micrometers, the average elastic modulus (GPa/micrometer) of the part which will consist of an organic protective coat and a stress relaxation layer supposing it is 3GPa(s) is set to (3x10+1x50) / 60**1.3, and, on the other hand, the thickness of a stress relaxation layer of the average elastic modulus of the ramp in Part A is [the elastic modulus / the elastic modulus] 1 at 50 micrometers. Therefore, with such structure, it will distribute into the part in which the organic protective coat was formed from the periphery, and the thermal stress of a stress relaxation layer can prevent breakage of the bump in the periphery which thermal stress originally concentrates. In addition, it is not necessary to necessarily have a particle in a stress relaxation layer, and even when not distributing a particle during a paste, minimum viscoelastic property required for printing should just be secured. However, when not distributing a minute particle during a paste, the margin of the various conditions in connection with printing may become extremely narrow.

[0040] The fourth process is explained succeedingly. In this example, wiring 4 for rewiring was made two-layer [of electrolytic copper plating and electric nickel]. In addition, the end of the wiring 4 for rewiring may be used also [pad / 3 / bump]. Although here showed how copper and nickel form a conductor using electroplating, it is also possible to use nonelectrolytic plating.

[0041] First, the electric supply film 16 for carrying out electroplating is formed all over a semiconductor wafer. Here, although it was possible to have used vacuum evaporationo, non-electrolytic copper plating, CVD, etc., the bond strength with a protective layer 8 and the stress relaxation layer 5 decided to use a strong spatter. As pretreatment of a spatter, in order to secure the flow between a bonding pad 7 and wiring 4 conductor for rewiring, sputter etching was performed. As spatter film in this example, the multilayers of chromium (75 nanometers)/copper (0.5 micrometers) were formed. The function of chromium here is to secure adhesion of the copper, stress relaxation layer, etc. which are located up and down, and the thickness has the desirable minimum

which maintains those adhesion. When chromium thickness becomes thick, membrane formation time amount will increase, in addition to the problem that productive efficiency falls, a protective layer 8 and the stress relaxation layer 5 will be put to the plasma of the high energy condition generated in a spatter chamber over long duration, and there is a danger that the ingredient which forms these layers will deteriorate. In addition, although necessary thickness is changed by the conditions of sputter etching and a spatter, the membraneous quality of chromium, etc., it is 0.5 micrometers at the maximum in general. In addition, it replaces with the chromium film used by this example, and the titanium film, titanium / platinum film, and a tungsten can also be substituted. On the other hand, when the electrolytic copper plating and electric nickel plating which are performed at a next process are performed, the minimum thickness of the thickness of spatter copper which thickness distribution of the plating film does not produce is desirable, and it determines the thickness which does not induce thickness distribution after also taking into consideration the amount of film decreases in acid washing performed as plating pretreatment. In the case of the copper thickness exceeding 1 micrometer, when thickness of spatter copper is made thick beyond the need, spatter time amount becomes long, in addition to the problem that productive efficiency falls, long duration etching is not avoided in the case of etching removal of the electric supply film 16 carried out at a next process, but side etching of the wiring 4 for rewiring becomes large as the result. By simple count, in etching the 1-micrometer electric supply film, also in wiring, 2-micrometer etching takes place on 1 micrometer of one side, and both sides. In actual production, since carrying out over etching is generally performed so that the etching remainder of the electric supply film may not occur, when etching the 1-micrometer electric supply film, side etching of about 5 micrometers of the wiring will be carried out. If side etching becomes large in this way, wiring resistance becomes large, or it will become easy to induce an open circuit and will be easy to generate a problem in the viewpoint of the wiring engine performance. Therefore, the thickness of spatter copper becomes 1 micrometer at the maximum in general.

[0042] Next, the reverse pattern configuration 17 of the wiring 4 for rewiring is formed using a resist using a phc lithography techniques. The thickness of the resist in the edge section of the stress relaxation layer 5 shown by B in drawing 4 becomes thick by the resist which flowed out of the slant surface part compared with other locations. For this reason, the negative mold is more desirable in order to secure resolution. As a resist, when a liquefied resist is used, resist thickness tends to become thin and there is an inclination for resist thickness to ten to become thick conversely, in the slant-face lower part in the slant-face upper part of the edge section of the stress relaxation layer 5 shown by B in drawing 4 . Large development tolerance is needed for carrying out patterning of the resist from which thickness differs in the slant-face upper part and the slant-face lower part on the same same light exposure and development conditions. Generally, since the negative-mold sensitization property resist was larger than a positive type sensitization property resist, the development tolerance to thicknes used the liquefied resist of a negative mold in this example. In addition, in using a film resist, since it does not generate, ****** in the slant-face upper and lower sides becomes usable also with a negative mold or a positive type, but since a slant surface part will be exposed from across and the real optical path length becomes long, if a negative mold is used also in this case, good results will be obtained in many cases. A negative mold is desirable especially when using a film resist with weak case where the inclination of the edge section of the stress relaxation layer 5 is large and breeching property. In this example, as shown in drawing 10 , the exposure mask 21 and the resist 22 stuck and the exposure machine of the type which has a clearance 20 in a part was used. The resolution limit in this exposure machine was about 10 micrometers in the case where the mask 21 for exposure and a resist 22 stick. According to our experimental result, the clearance 20 between the exposure mask 21 lowe parts and the relation of the wiring width of face to resolve came to be shown in Table 1. In addition, the value ir Table 1 changes with the ratios of the optical system and the development conditions of an exposure machine, th sensibility of a resist, resist hardening conditions, and wiring width of face / wiring spacing etc. The experimenta result shown in Table 1 is a value in case the ratio of wiring width of face / wiring spacing is 1.0.

[0043]

[Table 1]

表 1

		露光マスク下部の隙間 [μm]			
		40	60	80	100
配線幅 [μm]	15	×	×	×	×
	20	○	×	×	×
	25	○	○	○	×
	30	○	○	○	○
	40	○	○	○	○
	50	○	○	○	○

○：解像可
×：解像不可

[0044] Signs that a connection 23 and the bump putt 3 with an aluminum pad are connected to drawing 11 with the wiring 4 for rewiring are shown. In the case of the aligner used by this example, since the clearance between the lower parts of the exposure mask which is the axis of abscissa of Table 1 supports the thickness of a stress relaxation layer mostly, if the thickness of a stress relaxation layer is 60 micrometers, for example, the width of face of wiring is resolvable to 25 micrometers. Therefore, wiring width of face of a signal line can be made into 25 micrometers, and it can also wire by making wiring width of face of a power source or a grand line into 40 micrometers. Moreover, it is also possible to make thick a part of the signal line, using wiring of a signal line as 25 micrometers.

[0045] The wiring 4 for rewiring in near the ramp of the stress relaxation layer 5 is expanded and shown in drawing 12 . As mentioned above, since resist thickness served as an ununiformity near the edge section of the stress relaxation layer 5, there was an inclination which a underdevelopment tends to generate in the field. Signs that the underdevelopment has actually happened to drawing 13 in the edge part of the stress relaxation layer 5 are shown. In this example, it solved by improving a surroundings lump of a developer for this cure. When it illustrates more concretely, they are policies, such as changing a circuit pattern configuration, as shown in drawing 14 or drawing 15 .

[0046] Drawing 14 shows the case where drawing 15 makes thick wiring width of face of only the edge part of the stress relaxation layer 5 with bad definition for the case where wiring width of face is made thick from the connection 23 with an aluminum pad to near the summit of the stress relaxation layer 5. In addition, the wiring width of face in these drawing 14 and drawing 15 is determined in consideration of the resolving property shown in the thickness and Table 1 of the stress relaxation layer 5. How to cancel the development remainder by extending developing time as other solutions is also considered. Moreover, since light diffracts in respect of a mask, it may originate in a clearance 20 existing under the exposure mask 21, and a definition fall and a pattern precision fall may take place.

[0047] As a solution of this phenomenon, optical-system modification of (1) exposure machine, breeching nature amelioration of (2) resists, prebaking condition rationalization of (3) resists, (4) multistage exposure, etc. are raised. If one example is given about modification of the optical system of an exposure machine, the policy that NA value uses 0.2 or less or more 0.0001 exposure machine will be raised. The definition of a pattern and precision can be improved by combining suitably the device on the process of not only the example given here but well-known common use.

[0048] Since the edge section of the stress relaxation layer 5 has the description on the structure which the stress produced by the difference in the physical-properties value of a wafer and the stress relaxation layer 5 tends to concentrate, an open circuit can also be effectively prevented by making wiring thick by the ramp of the stress relaxation layer 5. In addition, you may make it change the width of face of wiring with a power source / grand line, and a signal line, as it is necessary to not necessarily make no wiring into the same size for example, and is shown in drawing 16 . In this case, when an electric property is taken into consideration, it is desirable to make a power source / grand line thicker than a signal line generally. It is because the capacity component which wiring

has by this increases and effect is done at the time of high-speed operation, when a signal line is made thick. Conversely, since the effectiveness that supply voltage is stabilized is expectable if a power source / grand line is made thick, it is desirable rather. Therefore, it is desirable to consider as the pattern which made the edge circumference thick so that it may illustrate, and only the part which stress concentrates can be eased at worst about wiring for signals, and to make a ramp thick uniformly about wiring for the object for power sources or glands. On the other hand, about the flat part in which the stress relaxation layer is not formed, signal wiring is made thin in consideration of the effect of the capacity component of wiring. However, it is necessary to take thi into consideration with the class of semiconductor device, or its circuit pattern each time. For example, although it is dependent also on a semiconductor device or its circuit pattern, since big effectiveness is in capacity reduction of wiring when the thickness of a protective coat 8 is increased, when signal wiring must be made thicl by the flat part in which the stress relaxation layer is not formed, it is desirable to form a protective coat 8 thickly When increasing wiring width of face 10%, specifically, it is desirable to also increase the thickness of a protective coat 8 about 10%. On the other hand, the wiring width of face in the up flat part of a stress relaxation layer receives a limit from signal-line capacity with a wiring consistency rather. That is, the upper limit of the wiring width of face in the up flat part of a stress relaxation layer is calculated from the alignment accuracy in th path of the wiring number which it lets pass at spacing of a bump pad, and a bump pad, and a wiring formation process etc. If an example is shown concretely, when bump pad spacing will pull 3 wiring between 300 micrometers of diameters of a pad, and a pad by 0.5 millimeters, it is (500-300) / (3x2-1) =40. It becomes the count to say. From this count result, they could be average wiring width of face / wiring spacing =40 micrometer by this example.

[0049] The fifth process is explained. In this example, copper plating was carried out using sulfuric-acid acidity copper-plating liquid. After electrolytic copper plating performed washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing, it connected the electric supply film 16 to cathode, and connected and carrie out the copper plate containing Lynn to the anode plate.

[0050] Then, electric nickel plating is performed. In addition, when washing by the surfactant, rinsing, washing by the dilute sulfuric acid, and rinsing are performed before electric nickel plating, there is an inclination for the electric nickel-plating film of good membraneous quality to be easy to be obtained. Electric nickel plating connected the electric supply film 16 to cathode, connected the nickel plate to the anode plate, and went. Although the nickel-plating bath of the gap which is not well-known common use of electric nickel plating suitable at this example could also be usable and the Watts bath system or the sulfamine bath system was sufficient as it, it was performed using the Watts bath system under the plating conditions adjusted so that platin film internal stress might become the proper range by this example. Although there is a fault that a sulfamine bath has the inclination which a plating liquid component tends to decompose a little an expensive top compared with a Watts bath, coat stress tends to control it. On the other hand, since coat stress generally tends to become large, a Watts bath has the fault that the danger that a crack will go into a wiring layer for the coat stress (tensile stress) which self has increases, when thick-film plating is carried out. Although the Watts bath was used in this example, when using a sulfamine bath, or when using a Watts bath, it is good to carry out, after carrying out beforehand the model experiment for asking for the proper range of whenever [class / of additive (coat stress inhibitor) / and concentration, plating current density, and plating solution temperature]. It carried out, after searching for beforehand the conditions from which these are controlled by this example proper, and a crack doe not go into wiring in 10 micrometers or less of thickness. In addition, plating membrane stress is one of the indexes in connection with the metallic crystal stacking tendency of depositing nickel, and in order to control growth of the solder diffusion layer mentioned later, it is necessary to control it proper. If membrane stress galvanizes under the conditions controlled proper, a plating coat will come to carry out the eutectoid of the mino constituent of the amount of specification. For example, in the case of the film containing 0.001 - 0.05% of sulfur, the content of a specific crystal orientation side increases. Speaking more concretely, the content sum tota of the orientation sides 111, 220, and 200 and 311** becoming 50% or more. The thickness of electric nickel plating determines an optimum value with the class and reflow conditions of the solder used at a subsequent process, and the product property (mounting gestalt) of a semiconductor device. What is necessary is just to determine that the thickness of the alloy layer of the solder and nickel which are formed in the case of a solder reflow or mounting repair will specifically become more than nickel-plating thickness. The thickness of the

above-mentioned alloy layer becomes so large [it is so large that the concentration of the tin in solder is high, and] that reflow upper limit temperature is high. Thus, when the nickel layer was formed after copper wiring as wiring for rewiring, wiring for rewiring receives deformation with the thermal stress committed between a semiconductor device and the circuit board and the stress is released after that, wiring for rewiring can return to the configuration before deformation by the spring nature of a nickel layer. For example, it deforms in the form which the wiring 4 for rewiring currently formed a stress relaxation layer and on it stuck to each other according to an operation of the thermal stress caused by actuation of a semiconductor device. The deflection part of the redundancy part of wiring for rewiring in the swelling part of a stress relaxation layer is used for deformation of wiring for rewiring at this time. Then, when it is released from thermal stress etc. and a stress relaxation layer returns to the original configuration, for wiring for rewiring, only in copper wiring, copper wiring is a pile to return in the original wiring configuration at own spring nature of copper wiring. On the other hand, if a nickel layer is formed after copper wiring, wiring for rewiring (copper wiring) can return to the original configuration easily by the spring nature of the nickel layer. In addition, being formed after copper wiring may have spring nature comparable as a nickel layer not only on a nickel layer but on copper wiring. Moreover, to form wiring which is elastic instead of copper wiring, a nickel layer is necessarily unnecessary.

[0051] At the sixth process, after performing electrolytic copper plating and electric nickel plating, the resist 17 which is the reverse pattern of wiring is removed, and the electric supply film 16 which formed membranes beforehand by carrying out etching processing is removed. Although there was a class of ferric chloride, alkali system etching reagent, etc. of copper etching, in this example, the etching reagent which uses a sulfuric acid/hydrogen peroxide solution as a principal component was used. If there is no etching time for 10 seconds or more, control will become difficult, and since it will also produce the problem that side etching becomes large or a baton becomes long in etching, for example exceeding 5 minutes if too much long time amount etching is performed although it is disadvantageous in a practical viewpoint, an etching reagent and etching conditions are good to ask by experiment suitably. By this example, the etching reagent which uses potassium permanganate and a meta-silicic acid as a principal component was used for etching of the chromium part of the electric supply film 16 carried out succeedingly. In addition, the above-mentioned electric nickel-plating film is functioning also as etching resist in the case of etching of the electric supply film 16. Therefore, it is good to take into consideration the etch selectivity of nickel, copper and nickel, and chromium, and to determine the presentation component of an etching reagent, and etching conditions. For example, speaking concretely, by the sulfuric-acid hydrogen-peroxide etching agent used in the case of copper etching, making the content of a sulfuric acid into 15% or less desirably 50% or less at the maximum. Thereby, copper can be etched by about 10-time etch selectivity to nickel.

[0052] At the seventh process, only the bump pad 3, the cutting section 24, and its perimeter formed the surface protective coat 6 which carried out opening, and formed gold in the bump pad section 3 by carrying out non-electrolyzed gilding succeedingly. Here, after using a solder resist as a surface protective coat 6 and applying this all over a semiconductor device 13, a pattern is formed in exposing and developing negatives. In addition, it is also possible to use ingredients other than a solder resist, such as photosensitive polyimide and polyimide for printing, and to form the surface protective coat 6. By passing through the above processes, the surface protective coat 6 will cover completely the wiring 4 for rewiring, the stress relaxation layer 5, a protective coat 8, etc. For this reason, the surface protective coat 6 can inhibit that the wiring 4 for rewiring, the stress relaxation layer 5, and a protective coat 8 deteriorate, exfoliate and corrode with the stimulative matter.

[0053] Even at this seventh process, the wiring 4 for rewiring from the aluminum pad 7 to the bump pad 3 and the bump pad 3 are formed, as shown on the wafer 9 with which the semi-conductor was formed at drawing 17 and drawing 2 .

[0054] At the eighth process, a bump is formed using solder ball loading equipment and a reflow furnace. That is, the flux and the solder ball of the specified quantity are carried on the bump pad 3 by using solder ball loading equipment. Under the present circumstances, temporary immobilization of the solder ball is carried out by the adhesion of flux on a bump pad. It is once fusing a solder ball and solidifying again after that in throwing into a reflow furnace the semiconductor wafer with which the solder ball was carried, and becomes the bump 1 linked to the bump pad 3 shown in drawing 1 . In addition, there is also the approach of forming a bump 1 by carrying out printing spreading of the soldering paste on the bump pad 3 using a printing machine, and carrying out a

reflow of this. Also in which approach, it becomes possible [a solder ingredient] to choose various things, and many of solder ingredients currently supplied to the commercial scene in this time can be used. In addition, although a solder ingredient is limited, it is using a plating technique and there is also the approach of forming a bump 1. Moreover, the bump who formed using the resin which blended the bump who used the ball which used gold and copper as the nucleus, and the electrical conducting material may be used.

[0055] By passing through the process from the first process to the ninth process, it has the stress relaxation laye 5 shown in drawing 1 , and the wiring 4 for rewiring is formed by the small routing counter, and the semiconductor device 13 with which the flection which stress moreover concentrates in the middle of the wiring 4 for rewiring does not exist can be realized. Moreover, pattern formation of the stress relaxation layer 5 which i an insulating layer of a thick film can be carried out by using a printing technique, without using exposure and a development technique, and the stress relaxation layer 5 can have a slant face for forming the wiring 4 for rewiring.

[0056] According to this example, even when under-filling is not carried out but flip chip bonding of the semiconductor device 13 is carried out, the connection dependability of a semiconductor device 13 improves sharply. For this reason, it turns out that the flip chip bonding which does not use under-filling in many electric products becomes possible according to this example, and it becomes possible to reduce the prices of various electric products. Furthermore, since under-filling is not carried out, removal of a semiconductor device 13 is attained. That is, when the semiconductor device 13 linked to the circuit board is a defective, it becomes possible to remove a semiconductor device 13 from on the circuit board, and to reproduce the circuit board, and it becomes possible to reduce the prices of various electric products also by this.

[0057] Next, the ingredient of the stress relaxation layer 5 concerning this example is explained. Although the ingredient for stress relaxation layer 5 formation used most suitably at this example is paste-like polyimide, not only this but conversion amide imide resin, ester imide resin, ether imide resin, polyester resin, conversion silicone resin, conversion acrylic resin, etc. are sufficient as it. In the resin which has imide association among the resin which carried out [above-mentioned] listing, for example, polyimide, amide imide, ester imide, and ether imide, it excels in a heat mechanical property, for example, the reinforcement in an elevated temperature etc., thanks to the firm frame by imide association, and ****** of the plating electric supply film formation approach for wiring spreads as the result. For example, the plating electric supply film formation approach accompanied by high temperature processing, such as a spatter, can be chosen. When it is resin with the part condensed in association other than imide association, such as silicone resin, acrylic resin, polyester resin, amide imide, ester imide, and ether imide, although a heat mechanical characteristic is inferior a little, it may be advantageous in respect of workability, a resin price, etc. For example, by polyester imide resin, generally, since curing temperature is lower than polyimide, it is easy to treat. In this example, a component property, a price, a heat mechanical characteristic, etc. are synthetically taken into consideration out of these resin, and these resin is used properly suitably. Two or more kinds are blended, a coupling agent, a coloring agent, etc. for improving an adhesive property with various interfaces to this are blended, and the ingredient for stress relaxation layer 5 formation can use [independent or] resin, such as epoxy, a phenol, polyimide, and silicone.

[0058] Although the elastic modulus of the stress relaxation layer 5 can apply the thing of 0.1 to 10.0GPa extent in a room temperature, what has an elastic modulus lower than common polyimide is desirable. In being too small, in case it performs the formation of a projection electrode and the functional test of this semiconductor device which are mentioned later by an elastic modulus being less than 0.1GPa(s), we become easy to deform a wiring part and are anxious about problems, such as an open circuit. Moreover, if the elastic modulus of the stres relaxation layer 5 becomes large exceeding 10.0G, the reduction effectiveness of sufficient stress will not be acquired, but we are anxious about the connection dependability at the time of carrying this semiconductor device in a substrate falling.

[0059] Furthermore, as for the curing temperature of the charge of stress relaxation layer 5 material, it is desirable to use the thing from 100 degrees C to 250 degrees C. It is because wafer stress increases by the heat shrink at the time of hardening cooling or there is concern from which the property of a semiconductor device changes, when management within the process at the time of semi-conductor manufacture is difficult and curing temperature becomes high from this when curing temperature is lower than this. Since the stress relaxation layer after hardening is exposed to various processes, such as a spatter, plating, and etching, properties, such as therma

resistance, chemical resistance, and solvent resistance, are also required. concrete -- as thermal resistance -- the glass-transition temperature (Tg) -- 150 degrees C -- super- -- it is desirable that it is 400 degrees C or less, and Tg is [180 degree C or more of Tg(s)] 200 degrees C or more most preferably more desirably. Drawing 41 is an experimental result which shows the relation between glass transition temperature (Tg) and coefficient of linear expansion. This shows that the crack has not occurred, if glass transition temperature (Tg) is 200 degrees C or more. In addition, the coefficient of linear expansion (alpha 1) in the field below [the viewpoint which stops the deformation in various temperature processings in a process to] Tg is so desirable that it is small. It is so good that it is specifically close to 3 ppm. Although a low spring material generally has a large coefficient of linear expansion in many cases, as for the range of the coefficient of linear expansion of stress relaxation layer 5 ingredient suitable at this example, it is desirable that it is the range of 3 ppm - 300 ppm. It is the range of 3 ppm - 200 ppm more preferably, and the range of the most desirable coefficient of linear expansion is 3 ppm - 150 ppm. On the other hand, as for pyrolysis temperature (Td), it is desirable that it is about 300 degrees C or more. When Tg and Td are less than these values, there is a danger that deformation of resin, and deterioration and decomposition will take place at a spatter or a sputtering etch process as the heat process in the inside of a process. When it says from a chemical-resistant viewpoint, it is desirable for resin deterioration of discoloration, deformation, etc. not to take place 30% by the immersion of 24 hours or more to a sulfuric-acid water solution or 10% sodium-hydroxide water solution. As solvent resistance, it is desirable to set a solubility parameter (SP value) to 8-20(cal/cm3) 1/2. When the object for the stress relaxation layers 5 is the ingredient which comes to carry out conversion of some components to base resin, it is desirable for the greater part of the presentation to have said the range of the above-mentioned solubility parameter. Speaking more concretely, it being desirable fo less than 8 and a 20 super-****** component not to contain [the solubility parameter (SP value)] more than 50 % of the weight. When such chemical resistance and solvent resistance are insufficient, an applicable manufacture process may be limited and it is not sometimes desirable from a viewpoint of manufacturing cost reduction. After taking into consideration synthetically actually the ingredient cost and the process degree of freedom with which are satisfied of these properties, it is good to determine the ingredient for stress relaxation layer 5.

[0060] Then, the relation between the thickness of a stress relaxation layer, wafer stress, and alpha rays is explained. Drawing 18 shows the thickness of a stress relaxation layer, and the relation of wafer stress. When diameter the wafer of 8 inches is made to apply and harden a stress relaxation layer, if thickness becomes thick rather than 150 micrometers, wafer stress becomes large, and as shown in drawing 18 , the crack of a wafer, peeling of an insulator layer, etc. will become easy for the curvature of a wafer to become large or to generate it.

[0061] On the other hand, the relation between the thickness of a stress relaxation layer and the amount of alpha rays which penetrates the inside of a stress relaxation layer was shown in drawing 19 . It generates by collapse of uranium, thorium, etc. which are contained as an impurity in the solder used for a semiconductor device, and alpha rays cause malfunction of the transistor section. If the thickness of a stress relaxation layer becomes thicke than 35 micrometers as shown in drawing 19 , alpha rays will hardly be penetrated, and the problem of malfunction by alpha rays is not produced. Since alpha rays will penetrate if the thickness of a stress relaxation layer becomes thin from 35 micrometers on the contrary, it turns out that malfunction by alpha rays becomes easy to take place.

[0062] Connection dependability with the substrate in which it prevented that alpha rays reached to the circuit part formed in the semiconductor device front face from these relation by making thickness of a stress relaxation layer into 35 micrometers or more 150 micrometers or less, and a semiconductor device and this were carried is securable. In addition, the part which cannot be easily influenced [the memory cell 110 grade which is easy to receive incorrect actuation of the part which is easy to be influenced of alpha rays depending on the configuratio of a semiconductor device, for example, a transistor, and] of alpha rays is in the same component. Then, it can prevent that alpha rays reach to the circuit part formed in the semiconductor device front face by making thickness of a stress relaxation layer into 35 micrometers or more 150 micrometers or less to the part which is [as opposed to / especially / alpha rays] easy to be influenced, as shown in drawing 20 and 21. In addition, even if it makes it less [the thickness of the stress relaxation layer formed in the field which cannot be easily influenced of alpha rays] than 35 micrometers, it is satisfactory in the viewpoint of alpha-rays electric shielding. As it follows, for example, is shown in drawing 21 , alpha-rays electric shielding forms the stress relaxation laye

of a required field thickly, in other fields, a stress relaxation layer can be formed thinly, and average thickness of the whole stress relaxation layer can also be made into 35 micrometers or more 150 micrometers or less. When giving such a device, it is desirable to consider as the configuration of the semiconductor device which took into consideration the magnitude of the thermal stress strain concerning each bump. Since such a stress relaxation layer thicker [be easy to receive a thermal stress strain and] that it generally goes to the periphery of a semiconductor device 13 is needed, it is good to arrange the transistor field which is easy to be influenced to alpha rays on the periphery of a semiconductor device 13, and to arrange the field which cannot be easily influenced to alpha rays near the center of a semiconductor device 13. For example, as shown in drawing 38 , it i also possible to make thickness of the stress relaxation layer 5 so gradually thick [near the center of a semiconductor device 13 is thin, and] that it go to the periphery section. In this case, since a connection angle becomes small while connection height becomes large compared with other bumps, the bump's herself stress relaxation function increased and the bump near a center has substituted for the stress relaxation function of the stress relaxation layer 5 which became thin. In addition, as shown at drawing 39 in the case of the semiconductor device 13 which has the field which is not influenced at all of alpha rays, as long as it arranges the field which is not influenced of alpha rays near the center of a semiconductor device 13, the stress relaxation layer 5 may not b formed near the center of a semiconductor device 13. Next, the example of the stress relaxation layer which includes the particle from which a stress relaxation layer and a presentation differ as other examples is explained

[0063] The particle contained in the stress relaxation layer 5 mentioned above is the same ingredient as the stress relaxation layer 5, and has the same physical properties. It can have viscoelastic property required for printing because a particle distributes in a stress relaxation layer.
[0064] However, with this structure, since a physical-properties value changes rapidly on the boundary of a wafe and the stress relaxation layer 5, thermal stress etc. may concentrate on that boundary part, and wiring may carry out an open circuit etc.
[0065] Then, the property of the stress relaxation layer 5 formed on the circuit forming face of a wafer is change in the thickness direction, and it was made for the property of the stress relaxation layer by the side of a wafer front face to become close to the property of a wafer in this example.
[0066] The open-circuit prevention of the wiring section of the stress of the force discontinuous to wiring which lessened the difference of the property in the boundary section a wafer top face and under a stress relaxation layer, and established it on these by this, the tension by expansion contraction of a stress relaxation layer, or compression and bending is attained by making it not join the wiring section.
[0067] Furthermore, the substrate side with which the property of the stress relaxation layer 5 by the side of a wafer carries near and this semiconductor device in a wafer is effective not only in wiring on the stress relaxation layer 5 but the improvement in a connection life of the connection of this semiconductor device and said substrate by carrying out near to the property of the substrate.
[0068] Here, a coefficient of thermal expansion or an elastic modulus can be considered as a property of changing gradually in the thickness direction of the stress relaxation layer 5. And as a concrete means to change the property of a stress relaxation layer, as shown in drawing 22 , the silica particle 102 which is an insulating particle is blended, distribution of the loadings of the silica particle 102 is given in the thickness direction of the stress relaxation layer 5, and a coefficient of thermal expansion and an elastic modulus are changed gradually. In the part over which many silica particles 102 are distributed, an elastic modulus becomes [the coefficient of thermal expansion of the stress relaxation layer 5] small highly. On the other hand, if the loadings of the silica particle 102 decrease, a coefficient of thermal expansion will become large and an elastic modulus will become low.
[0069] By performing distribution of the circuit formation on a wafer, the stress relaxation stratification, and a silica particle, wiring formation on a stress relaxation layer, etc. in the state of a wafer, there are little simplification of a whole process, variation at the time of manufacture, etc., and the improvement in a life of the wiring section is possible also for the production process of the semiconductor device in this example.
[0070] In this example, one kind or the particle which blends two or more kinds and consists of organic materials, such as polyimide and silicone, if needed may be suitably blended for the particle which consists of inorganic materials, such as the silica and alumina which are an insulating particle for adjusting an elastic

modulus and heat expansion to the stress relaxation layer 5, and boron nitride.
[0071] Furthermore, since malfunction by the ultraviolet rays of the circuit section formed on modifiers, such as thermoplastics which raises the elongation after fracture and the breaking strength of the coupling agent and the resin which consists of alkoxysilane, titanate, etc. for adhesive improvement with the various interfaces which constitute a silica particle and an insulating resin layer, and a wafer etc. prevents, it is possible to also blend the hardening accelerator for promoting the hardening reaction of the color for coloring an insulating resin layer, a pigment, and a resin layer etc.
[0072] As the formation approach of the stress relaxation layer 5 of having changed the property in the thickness direction, the liquefied stress relaxation layer 5 which comes to blend the ingredient of said publication, for example is applied on the circuit side of a wafer, it is the process which carries out heat hardening of this stress relaxation layer 5, and there is a method of make the insulating particle which consists of a blended silica sediment gradually to a wafer side. If a particle with smaller particle diameter cannot sediment easily early, sedimentation turns a wafer down and a particle with larger particle diameter performs heat hardening of a stress relaxation layer when the particle diameter of a silica particle has distribution, distribution of a property will be formed in the thickness direction of a stress relaxation layer.
[0073] As an approach of controlling concentration distribution in the direction of thickness of the silica particle blended with the stress relaxation layer 5, the curing temperature of insulating resin and a curing temperature profile are adjusted suitably, or there is a method of changing the particle size distribution of insulating particles, such as an approach, a silica particle, etc. which blend suitably the reaction inhibitor for delaying the loadings of the hardening accelerator for bringing advance of hardening forward, a class, or hardening etc.
[0074] A silica particle applicable to this example can apply what fused and crushed the lump of the ingot-ized silica, the thing which carried out heating fusion and conglobated the silica particle again after crushing a silica ingot, the silica particle compounded further. The particle size distribution and loadings of a silica particle can be variously changed according to the magnitude of the semiconductor device which applies the structure of this example, thickness, a degree of integration, the thickness of the stress relaxation layer 5, and the particle size of a particle and the class of substrate to carry.
[0075] When forming the stress relaxation layer 5 by print processes, it may be necessary to change distribution of particle diameter also with the dimension of the mask applied depending on the approach of printing.
[0076] In addition, the stress relaxation layer 5 does not need to be formed by one printing, and as shown in drawing 23 , it may be formed by at least two printings or more. Furthermore, the loadings of the silica particle contained in each layer are changed, and you may print.
[0077] In this example, since the physical properties of the part in which wiring is formed do not change from the circuit section of a wafer rapidly in the phase of resulting in the electrode prepared on the stress relaxation layer, the big force does not concentrate on some wiring and open-circuit prevention of wiring is attained.
[0078] Next, an example of the example of the semiconductor device 13 which made thin thickness of the stress relaxation layer 5 of bump 1 directly under which exists in the circumference approach of a semiconductor device 13 compared with other parts is explained using drawing 24 . As for bump 1a of the outermost periphery, only in delta, in this example, height is low compared with bump 1b of that one inside.
[0079] There is a method of changing the rate of the solvent under printing conditions, such as existence of the minute particle contained in stress relaxation stratification ingredients, such as a paste-like polyimide ingredient, a configuration of a particle, combination and a print speed, a version detached building rate, and a count of printing, and paste etc. as an approach of making thickness of the stress relaxation layer 5 thin about the periphery of a semiconductor device 13.
[0080] In bump 1a which generally exists in the circumference approach of a semiconductor device 13, a big distortion has arisen compared with other bump 1b etc. with the various loads after connecting a semiconductor device 13 to the circuit board 14. For example, since the coefficient of linear expansion of a semiconductor device 13 and the circuit board 14 differs, at the time of a temperature rise, such a big distortion generates them that it is set to bump 1a of the circumference approach of a semiconductor device 13. When this distortion is large, or when carrying out a repeat operation, it is easy to destroy bump 1a from the circumference of a semiconductor device 13.
[0081] as [showed / the bump 1 / when thickness of the stress relaxation layer 5 was made thin about the

circumference approach of a semiconductor device 13, and it became possible to control the configuration of the corresponding bump 1 of a part and connected with the circuit board 14 / as it was in this example, / drawing 25 -- longwise -- it is set to bump 1aa. such -- longwise -- in bump 1aa, since the volume itself is the same as that of the other bumps 1, the contact angle of a bump 1 and the bump pad 3 and the contact angle of a bump 1 and the pad on the circuit board 14 become large. That is, it is set to alpha1>alpha2 and beta1>beta2 in drawing 25 .
[0082] The stress concentration to the connection of a bump and Bud will be eased because a contact angle becomes large. Thus, the connection dependability of a semiconductor device 13 and the circuit board 14 can be raised by making thickness of the stress relaxation layer 5 thinner about the bump pad 3 formation part of the periphery of a semiconductor device 13 than other parts, and making a bump's 1 configuration longwise. In addition, the cross-section configuration of the stress relaxation layer 5 can be designed within limits which do not have trouble at the time of connection of as opposed to the circuit board 14 of a semiconductor device 13 in a bump's 1 height, and can consider various things.
[0083] The magnitude of delta is determined in consideration of the bump height variation allowed value at the time of the functional test of the stress relaxation characteristic required of aa and the longwise bump 1(2) semiconductor device 13 which are located in the (1) outermost periphery, the bump height variation allowed value at the time of the connection to the circuit board 14 of the (3) semiconductor device 13, etc. If it describes more concretely, the above-mentioned stress relaxation characteristic can be found from the elastic modulus of the stress relaxation layer 5, and the size of a semiconductor device 13. On the other hand, about the variation at the time of a functional test and connection, after also taking into consideration deformation of a solder ball and the stress relaxation layer 5, those allowed values are calculated. For example, if a functional test pushes an inspection fixture from a bump top face and is made to deform the stress relaxation layer 5, it can carry out a functional test in the condition that bump height variation does not exist substantially. Even if it performs such actuation, since the modulus of elasticity is fairly low compared with a solder bump ingredient, rather than deformation of a solder bump, deformation of the stress relaxation layer 5 gives priority to the stress relaxation layer 5, it happens, and a blemish is not attached to a solder bump. So, even if the value of delta demanded from a stress relaxation characteristic becomes larger than the bump height variation demanded with functional test equipment, if it is the range which can respond according to deformation of the stress relaxation layer 5, it will not interfere. Moreover, since a stress relaxation ingredient is an elastic body, and a configuration is restored after inspection termination, there is no special problem also at the time of connection with a substrate. A consideration of this will determine (3) to the above (1) and delta as a matter of fact. As mentioned above, since, as for a stress relaxation characteristic, 35 thru/or a good result are obtained for the thickness of the stress relaxation layer 5 by 150 micrometers, it becomes delta=150-35=115 micrometer from a stress relaxation characteristic. Moreover, the value of delta= 115 micrometers is almost equal to the upper limit to the circuit board 14 permitted in the case of connection. Therefore, the value of delta turns into a upper limit, when 115 micrometers is many.
[0084] Moreover, detailed-ization of a semiconductor device progresses, and on the relation of wiring of a semiconductor device, the structure of this example can be adapted, also when a bump must be formed in the ramp of a stress relaxation layer. In addition, although the thickness of the stress relaxation layer 5 is controlled by above-mentioned drawing 24 in order to distinguish between height by outermost periphery bump 1a and bump 1b of the one inside, there is also an approach by the structural adjustment of a protective layer 8 as the other control approaches. For example, as shown in drawing 40 , the organic layer of a protective coat 8 is not formed directly under outermost periphery bump 1a, or it limits for forming very thinly, and inside bump 1b, there is the approach of forming the organic layer of a protective coat 8 more thickly. A problem does not have attaining the desired height difference delta in any way by adjusting suitably the thickness of the stress relaxation layer 5, and the organic bed depth of a protective layer 8, and controlling them if needed,, either.
[0085] Moreover, since external force tends to join the bump located in the outermost periphery of a semiconductor device and a crack etc. may be made to solder, some may be used as a buffer member among the bumps located in the outermost periphery. In this case, as for the bump who uses it as a buffer member, it is desirable to consider as an unnecessary thing, when the semiconductor device which is not electrically connected with the aluminum pad 7 operates electrically. A period until fracture occurs by the bump of required others when a semiconductor device operates electrically by this is extensible. In addition, about some bumps who

consider as a buffer member, enlarging the diameter of a bump can also extend the period to bump fracture further. In addition, in this example, in order to enlarge the suitable diameter of a bump, which approach of well-known common use may be used, but when one suitable approach is illustrated especially, the volume of solder itself is enlarging a bump land (pad), making it the same as that of other bumps. While the diameter of connection becomes large by enlarging a pad, since it is the same as others, bump height becomes low, as the result, the contact angle of a bump and a pad becomes large and the volume of solder can avoid the stress concentration to the point of contact of a pad with a bump, when it connects with the circuit board 14. Since the absolute value of crack die length when the diameter of a bump increased, until it results in fracture itself is large while crack progress within solder becomes slow, when stress concentration was lost, a bump contributes to the period extension to a stage greatly.

[0086] Moreover, if it thinks from a viewpoint of making easy the design of the wiring drawer of the circuit board which connects a semiconductor device It is desirable to arrange a power source or a grand line near the center of a semiconductor device. As the result As for the wiring 4 for rewiring which connects a bump pad with a near distance from the aluminum pad 7 and an aluminum pad as shown in drawing 26 (a) and (b), it is [the wiring 4 for the maximum wiring which connects a far bump pad as a signal line] desirable to use as a power source or a grand line. In this case, the bump with a near distance from an aluminum pad may be located in the ramp of the stress relaxation layer 5. Moreover, a power source or a grand line may be made to make wiring width of face larger than a signal line.

[0087] Other examples of a semiconductor device are shown in drawing 27 . At this example, the stress relaxation layer 5 is formed, where the semiconductor device 13 of the next door on the wafer 9 with which the semi-conductor was formed is straddled. The device on a design is made so that, as for the aluminum pad 7, the bump pad 3, and the wiring 4 for rewiring that connects these, the wiring 4 for rewiring may not cross the boundary of a semiconductor device 13 and the next semiconductor device 13. Although the production process is fundamentally [as what was already explained] the same, there is a difference after the seventh process.

[0088] In case a semiconductor wafer is cut, cutting of the stress relaxation layer 5 is also needed, but since the stress relaxation layer 5 is a low spring material, it is difficult for bundling up with the wafer 9 with which the semi-conductor with which most consists of silicon and reinforcement differs was formed, and cutting. For this reason, after performing cutting to the stress relaxation layer 5 first, the dicing of the wafer 9 with which the semi-conductor was formed is carried out. Hereafter, it explains using drawing 28 .

[0089] First, only the stress relaxation layer 5 is cut at the seventh amelioration process. It is good to use the rotary knife suitable for cutting of a low elastic resin ingredient as a cutting process. In addition, carbon dioxide gas laser, sandblasting, etc. can be used.

[0090] In the eighth amelioration process, a solder resist is applied to the whole surface as a surface protective coat 6. Printing and curtain coating using the mask of the shape of a mesh besides a spin coat method as the method of application are sufficient. Also in order to apply a solder resist, the wall surface of the cutting section of the stress relaxation layer 5 in the seventh amelioration process is not perpendicular, and it is desirable to mak it become the shape of reverse Ha's character. By performing this coating after cutting of the stress relaxation layer in the seventh amelioration process, the stress relaxation layer 5 can become the factor which exfoliates from the front face of a wafer 9 in which the semi-conductor was formed, or invasion of foreign matters, such as ion which causes the performance degradation of a semi-conductor, can be mitigated, and the device which secured endurance etc. can be offered.

[0091] In the ninth amelioration process, the pattern of the surface protective coat 6 is formed by performing sensitization development. Thereby, only the bump pad 3, the cutting section 24, and its circumference are exposed from the surface protective coat 6. Moreover, gold is formed on the bump pad 3 by giving non-electrolyzed gilding by using the surface protective coat 6 as a mask. In addition, although considered only as gilding in the example, you may give, before plating the plating of palladium or platinum with gold, and even if performs tinning after gilding termination, there is no special problem.

[0092] In the tenth amelioration process, the wafer 9 with which the semi-conductor was formed of dicing is divided into a semiconductor device 13. In addition, generally dicing is performed using a rotary knife.

[0093] Manufacture of the semiconductor device 13 which includes the process which cuts the stress relaxation layer 5 according to the above process is attained.

[0094] According to this example, even when the dimension of a semiconductor device 13 is small, it becomes possible to form the stress relaxation layer 5 satisfactory. In specifically forming the stress relaxation layer 5 ranging over two adjacent semiconductor devices Even if a dimension becomes half mostly, it is not necessary tc change the membrane formation technique of the stress relaxation layer 5. Even if it changes the magnitude of a semiconductor device by adjusting the width of face of the cutting section 24 which is cutting at the time of separating the configuration of a semiconductor device, a dimension, and the semiconductor device 13 of each other, and a configuration, manufacturing using the same printing mask may even become possible. Moreover, since the wiring 4 for rewiring has connected the aluminum pad 7 and the bump pad 3 through the ramp of the stress relaxation layer 5 like the first example, stress raisers do not exist in the wiring 4 for rewiring, either, but the flip chip bonding of it which does not need under-filling becomes possible.
[0095] In addition, especially the structure concerning this example can be adapted for the semiconductor device with which the pad was arranged by the pin center,large part of a semiconductor device, for example, DRAM etc

[0096] Moreover, although the stress relaxation layer 5 over two adjacent semiconductor devices 13 was cut in drawing in this example, as long as the slope section for the wiring 4 for rewiring to result [from the aluminum pad 7] in the bump pad 3 exists, it is also possible to adopt the structure where the stress relaxation layer 5 connected about the semiconductor device 13 of at least 2 more than, for example, four semiconductor devices which adjoin each other mutually, is cut. The connected stress relaxation layer 5 is formed and you may make it cut it about two trains which adjoin each other with a natural thing. In this case, since it becomes the process which can permit a location gap of the direction of a train, it is more applicable also to micro processing.
[0097] In each example, as shown, for example in drawing 2 or drawing 27 , it is good for the corner of the stress relaxation layer 5 to give a radius of circle. When it does not give a radius of circle, in case the stress relaxation layer 5 is printed using a paste-like polyimide ingredient, it sometimes gazes at the defect who involves in air bubbles. Moreover, the stress relaxation layer 5 becomes easy to exfoliate from a corner. If air bubbles remain in the stress relaxation layer 5, when a semiconductor device 13 is heated, air bubbles will explode and the fault of the wiring 4 for rewiring being disconnected will arise. For this reason, as for the corner of the pattern opening 1 of the metal mask for printing used for formation of the stress relaxation layer 5, rounding off is desirable.
[0098] In addition, using the metal mask for printing, or a dispenser, printing spreading of the stress relaxation layer 5 in each example can be carried out, and it can be formed.
[0099] Moreover, it can form approaches, such as sticking the resin sheet of not only the printing approach but a **********, air or blasting and the ink jet method using inactive gas, un-hardening, or a semi-hardening condition, or by combining these approaches suitably. When forming a stress relaxation layer by the printing approach, and the inclination of a printing section edge prints an insulating material and a printing mask is removed, in a heat hardening process, a flow of an insulating layer takes place at the end, and the ramp of an edge is formed. It is possible to create the edge which has a stress relaxation layer and a specific inclination per wafer by this approach by package. On the other hand, when forming a stress relaxation layer by the stamping, since the insulating material for stress relaxation is applied to the mold for ********** and the configuration of a stress relaxation layer is imprinted on a wafer, selection of the insulating material which form status change-ization of the edge at the time of insulating material hardening does not produce is attained. In this case, there is the description that the configuration of an edge tends to become fixed compared with a printing method. Furthermore, by the method which sprays an insulating material using gas etc., if those with a degree of freedom and nozzle dimensions are suitably chosen as the configuration at the time of the stress relaxation stratification ir order not to use a printing mask or ********** metal mold, in a printing mask or ********** metal mold, formation of the stress relaxation layer which is hard to form will be attained. Moreover, compared with a printing method or a ********** method, the thickness of a stress relaxation layer can be adjusted by adjustment of the amount of blasting, and the range of thickness adjustment also becomes large. By the method which sticks the resin sheet which is not hardened [semi-hardening or], in order to attain formation of the stress relaxation layer of a thick film and to use insulating sheet-like resin beforehand, there is the description of excelling in the surface smoothness of a stress relaxation layer front face. It becomes possible about these approaches to obtain desired stress relaxation layer thickness and an edge inclination a single or by combining suitably.

[0100] Next, other examples of a semiconductor device are shown. the cross-section schematic diagram showing the condition of having carried drawing 29 in the substrate for changing the projection electrode of a semiconductor device, and drawing 30 are the cross-section schematic diagrams showing the condition of having closed the clearance between a semiconductor device 13 and the substrate in which this is carried by resin 118 further -- it comes out.

[0101] The letter electrode 1 of a projection formed in the semiconductor device 13 is carried through a ********-strike or flux on the electrode 120 with which it corresponds on a substrate, melting of said letter electrode of a projection is carried out at a reflow furnace etc., and connection of a substrate 115 and a semiconductor device 13 is made. The substrate carrying a semiconductor device has the letter electrode 121 of a projection if needed [an electrode 120 and if needed] for carrying in the substrate used for various electronic equipment at the rear face of a semiconductor device loading side.

[0102] In case a semiconductor device 13 is carried in the substrate used for various electronic equipment, it is necessary to carry out heating melting of the letter electrode 121 of a projection prepared on the substrate 115. In order to raise further these mounting processes and the dependability in various trials, especially the dependability results over a drop impact test, between a semiconductor device 13 and substrates 115 is reinforced by resin 118.

[0103] The resin 118 filled up with between a semiconductor device 13 and a substrate 115 The liquefied epoxy resin used for the general semi-conductor closures, phenol resin, In order polyimide resin, silicone resin, etc. are usable and to adjust the coefficient of thermal expansion and elastic modulus of closure resin A silica, Or two or more kinds are blended. the particle which consists of inorganic materials, such as an alumina and boron nitride, - one kind -- Moreover, it is possible to blend the hardening accelerator for promoting the hardening reaction of the flame retarder for making the coupling agent and coloring agent which consist of resin, such as silicone and thermoplastics, alkoxysilane, titanate, etc. if needed, and fire retardancy give, or a fire-resistant assistant resin layer etc.

[0104] In this example, even if it is the case where the pitch of the letter electrode of a projection on a semiconductor device differs from the pitch of the electrode of the substrate used for various electronic equipment, it becomes possible by minding a predetermined substrate to connect with various electronic equipment.

[0105] In addition, also when you mount in the circuit board used for general electronic equipment like mounting to the substrate used as a semiconductor device, suppose that it is the same.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The fragmentary sectional view showing the structure of one example of the semiconductor device of this invention
[Drawing 2] The top view showing the condition that the semiconductor device of this example is formed continuously
[Drawing 3] Drawing having shown an example of the production process of the semiconductor device of this invention (1)
[Drawing 4] Drawing having shown an example of the production process of the semiconductor device of this invention (2)
[Drawing 5] Drawing having shown an example of the production process of the semiconductor device of this invention (3)
[Drawing 6] Drawing having shown the mask for printing used for formation of the stress relaxation layer of this invention
[Drawing 7] Drawing showing the process which is printing the stress relaxation layer
[Drawing 8] Drawing showing the version detached building process that a printing mask goes up from a wafer
[Drawing 9] Drawing having shown the semiconductor device with which the stress relaxation layer was formed
[Drawing 10] Drawing having shown the condition of having stuck the mask for exposure to the resist
[Drawing 11] Drawing having shown an example of wiring for rewiring
[Drawing 12] Drawing having shown another example of wiring for rewiring
[Drawing 13] Drawing showing the underdevelopment of the actual circuit pattern for rewiring
[Drawing 14] Drawing having shown another example of wiring for rewiring
[Drawing 15] Drawing having shown another example of wiring for rewiring
[Drawing 16] Drawing having shown another example of wiring for rewiring
[Drawing 17] Drawing having shown the semiconductor device which passed even through the seventh process in this invention
[Drawing 18] Drawing having shown the thickness of a stress relaxation layer, and the relation of stress
[Drawing 19] Drawing having shown the thickness of a stress relaxation layer, and the relation of alpha rays
[Drawing 20] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 21] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 22] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 23] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 24] Drawing having shown the semiconductor device which made thickness of a stress relaxation layer thin partially
[Drawing 25] Drawing having shown the condition of having connected to the circuit board the semiconductor device which made thickness of a stress relaxation layer thin partially
[Drawing 26] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 27] Drawing having shown the condition of having formed the stress relaxation layer ranging over the boundary of a semiconductor device and the next semiconductor device
[Drawing 28] Drawing having shown how to cut a stress relaxation layer

[Drawing 29] Drawing of one example which carried the semiconductor device in the substrate
[Drawing 30] Drawing of one another example which carried the semiconductor device in the substrate
[Drawing 31] Drawing having shown the conventional semiconductor device
[Drawing 32] Drawing having shown the condition of having connected the conventional semiconductor device to the circuit board
[Drawing 33] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 34] Drawing showing one another example of the structure of the semiconductor device of this invention
[Drawing 35] Drawing showing one another example of the structure of the semiconductor device of this invention
[Drawing 36] Drawing showing one another example of the structure of the semiconductor device of this invention
[Drawing 37] Drawing showing one example of the structure of the semiconductor device of this invention
[Drawing 38] Drawing showing one another example of the structure of the semiconductor device of this invention
[Drawing 39] Drawing showing one another example of the structure of the semiconductor device of this invention
[Drawing 40] Drawing showing one another example of the structure of the semiconductor device of this invention
[Drawing 41] Drawing showing the relation between glass transition temperature and coefficient of linear expansion
[Description of Notations]
1 [-- Bump pad,] -- A bump, 1aa -- A longwise bump, 2 -- Au plating, 3 4 [-- Aluminum pad,] -- Wiring for rewiring, 5 -- A stress relaxation layer, 6 -- A surface protective coat, 7 8 [-- Metal wiring,] -- A protective coat 9 -- The wafer, 10 in which the semi-conductor was formed -- A bump, 11 12 [-- Under-filling,] -- An insulating layer, 13 -- A semiconductor device, 14 -- The circuit board, 15 16 -- The electric supply film, 17 -- The reverse pattern of wiring, 18 -- The connection parts of an aluminum pad and wiring, 19 [-- Resist,] -- A boundary with a lower layer part, 20 -- A clearance, 21 -- An exposure mask, 22 23 -- A connection with an aluminum pad, 24 -- The cutting section, 25 -- The stencil made from a nickel alloy, 26 [-- A silica particle, 110 / -- A memory cell, 115 / -- A substrate, 116 / -- An electrode, 118 / -- Resin, 120 / -- An electrode, 121 / -- Electrode] -- A resin sheet, 27 -- A frame, 28 -- Pattern opening of a printing mask, 102

[Translation done.]

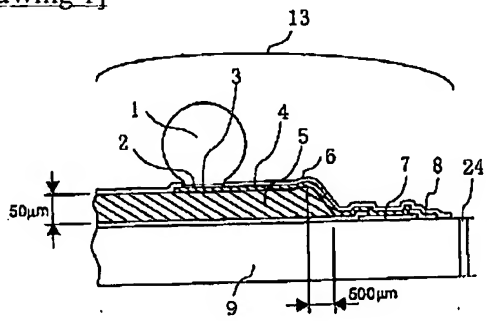
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

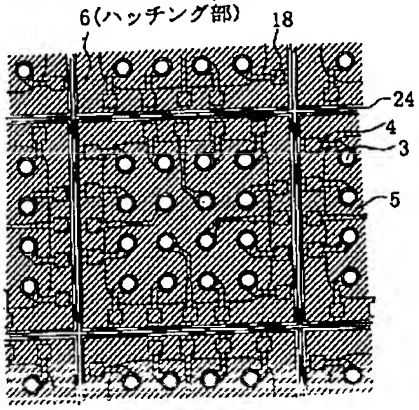
[Drawing 1]

図1



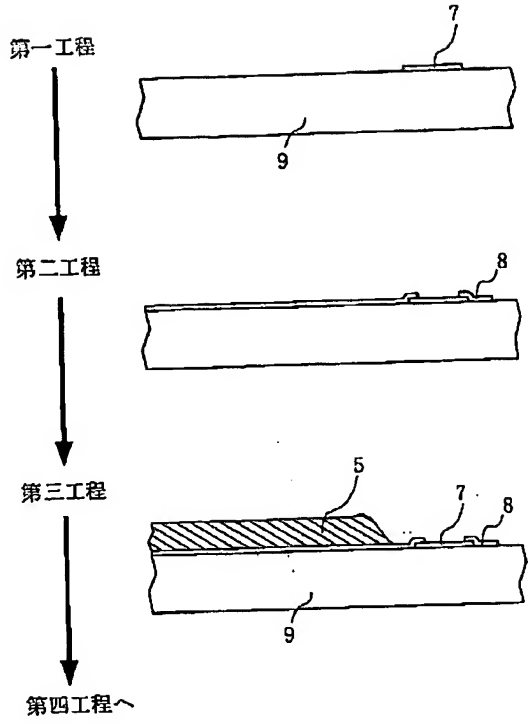
[Drawing 2]

図2



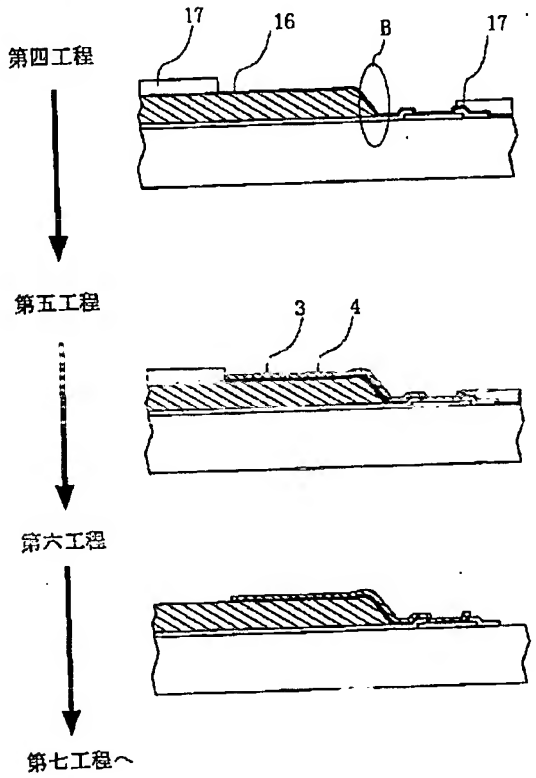
[Drawing 3]

図3



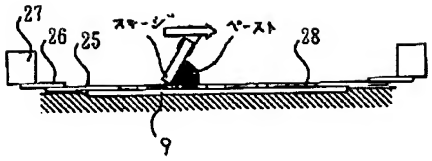
[Drawing 4]

図4



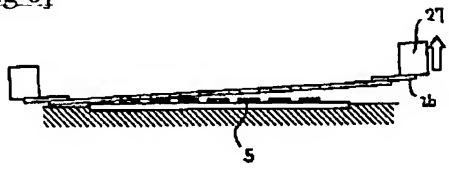
[Drawing 7]

図7



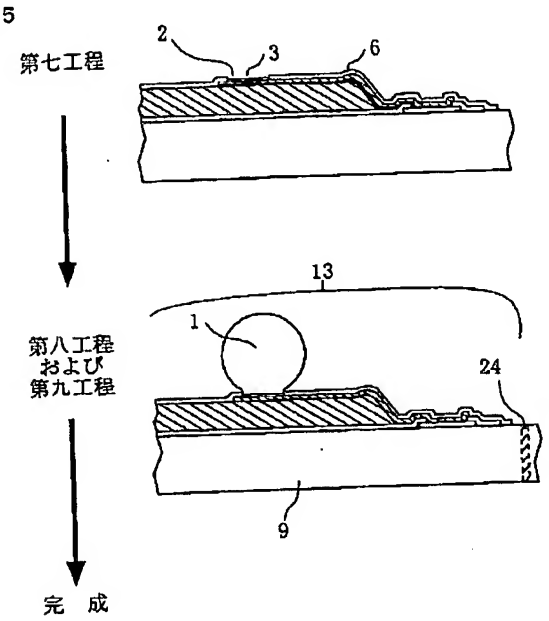
[Drawing 8]

図8



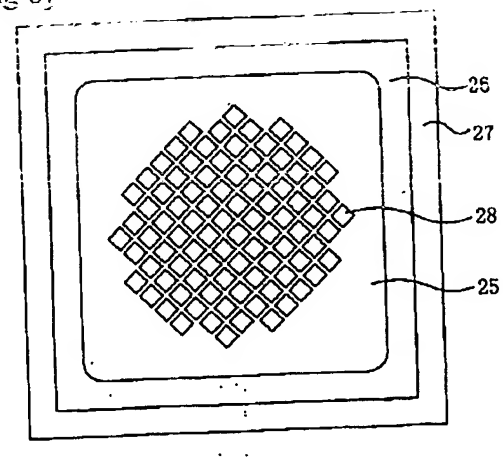
[Drawing 5]

図5



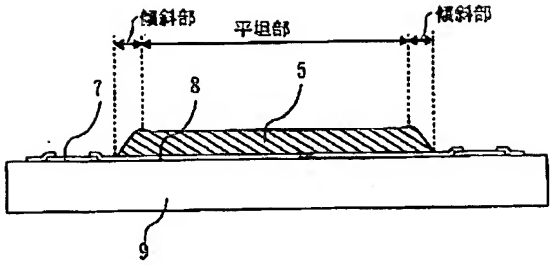
[Drawing 6]

図6



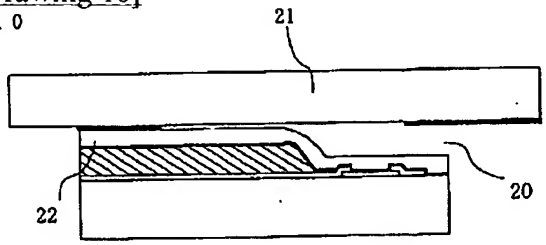
[Drawing 9]

図９



[Drawing 10]

図１０



[Drawing 11]

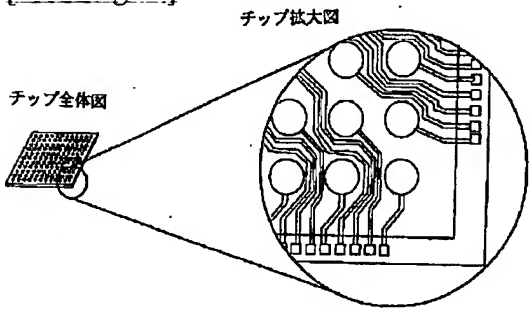
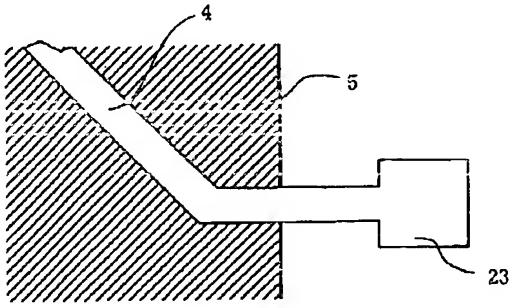


図 11

[Drawing 12]

図１２



[Drawing 13]

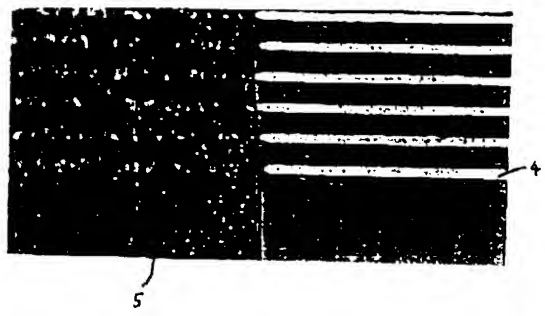
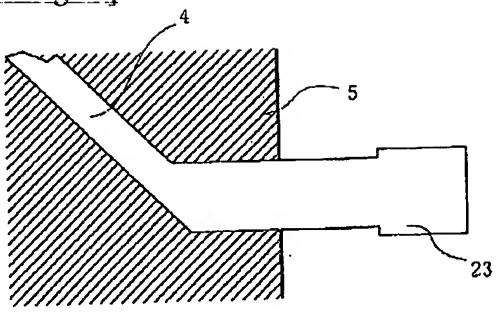


図１３

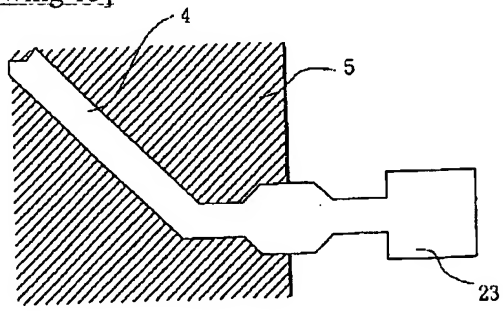
[Drawing 14]

図１４



[Drawing 15]

図１５



[Drawing 16]

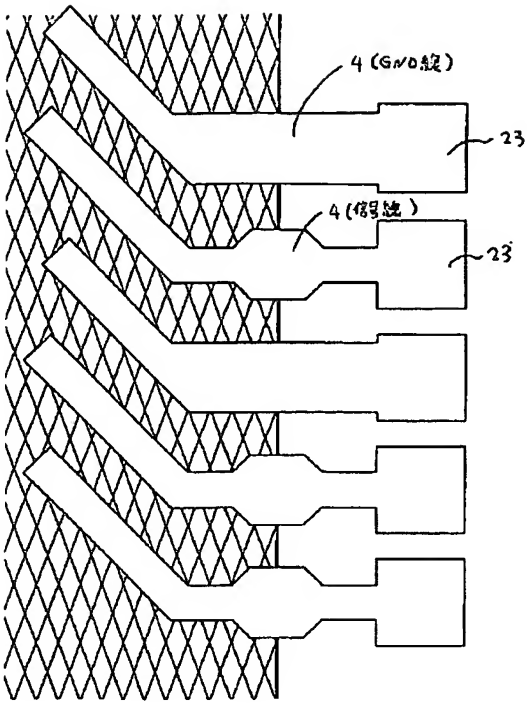
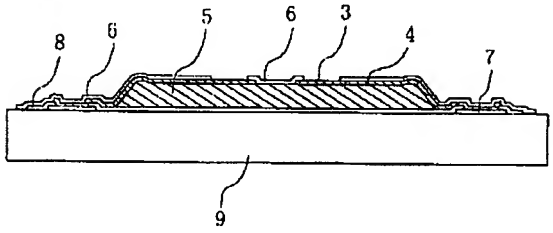


図16

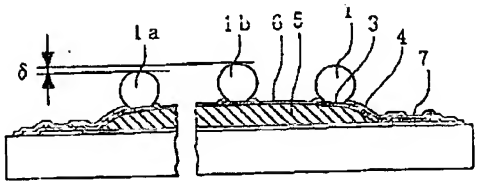
[Drawing 17]

図17



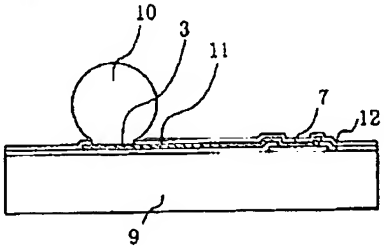
[Drawing 24]

図24



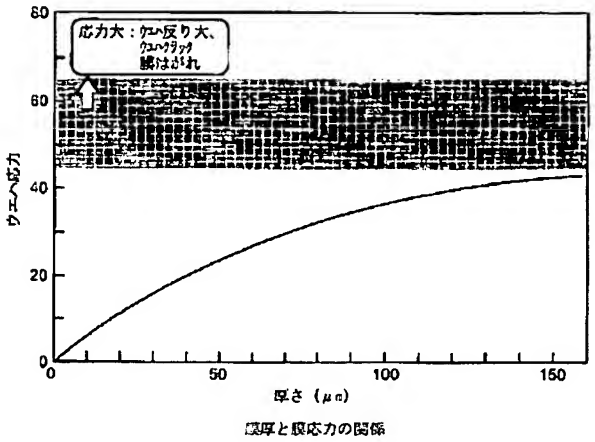
[Drawing 31]

図31



[Drawing 18]

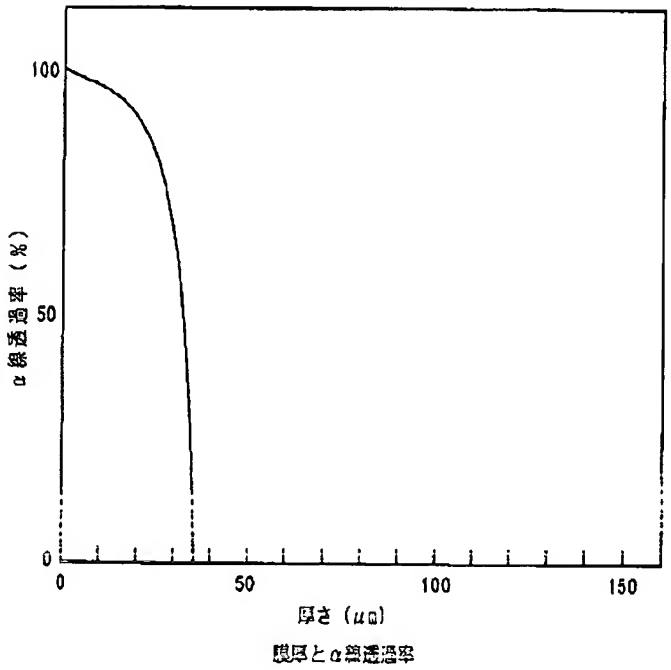
図１８



膜厚と膜応力の関係

[Drawing 19]

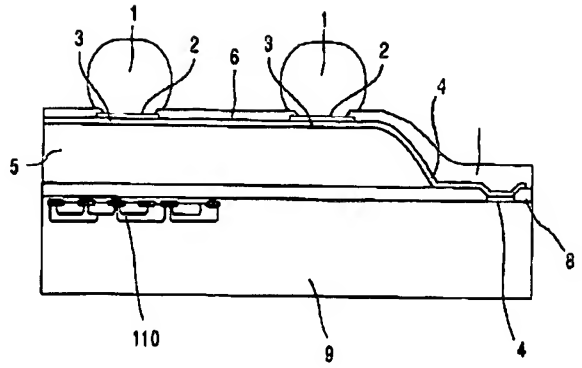
図19



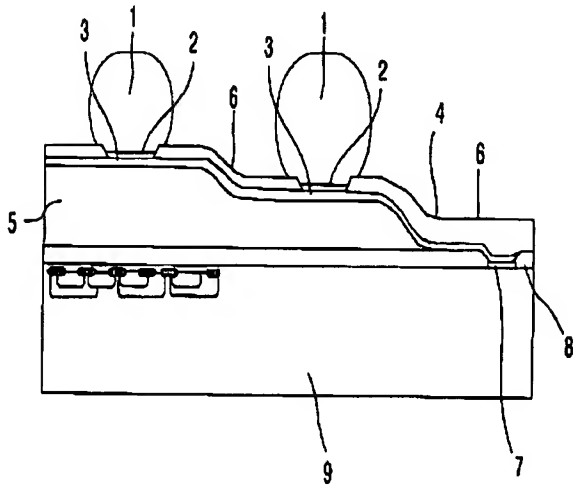
膜厚とα線透過率

[Drawing 20]

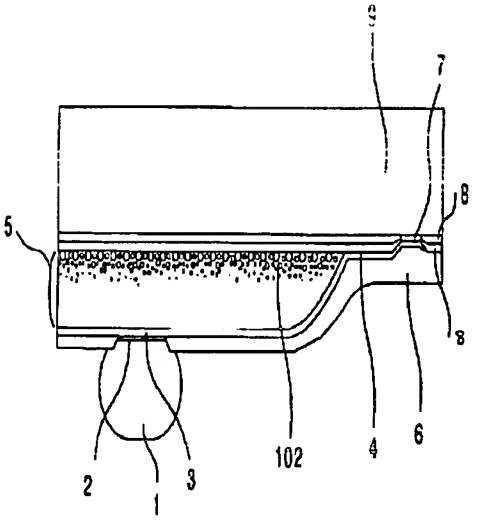
図20



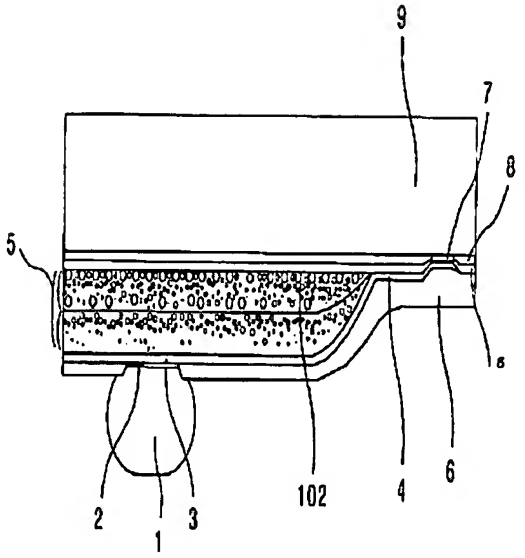
[Drawing 21]
図21



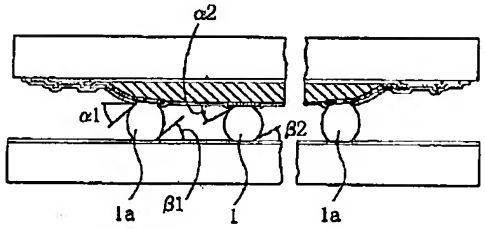
[Drawing 22]
図22



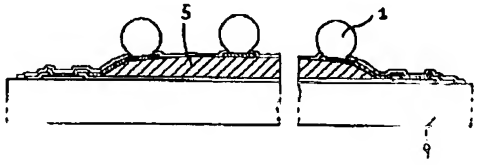
[Drawing 23]
図23



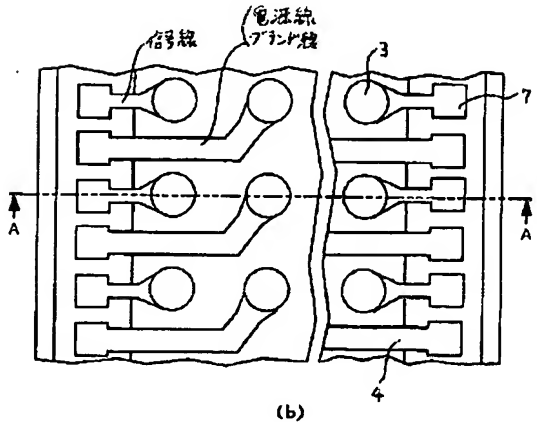
[Drawing 25]
図25



[Drawing 26]
図26



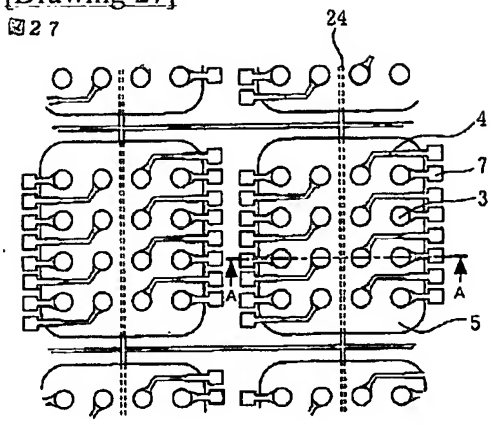
(a)



(b)

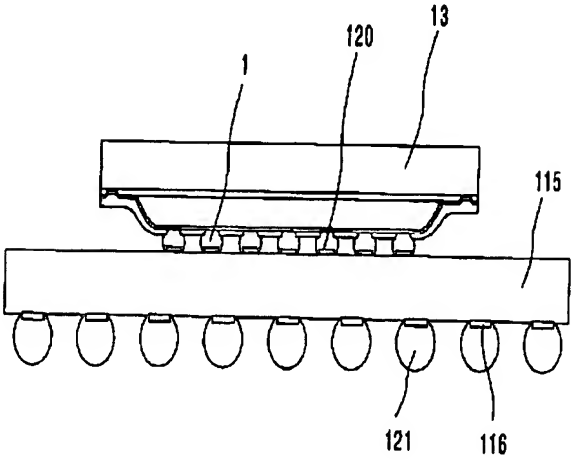
[Drawing 27]

図27



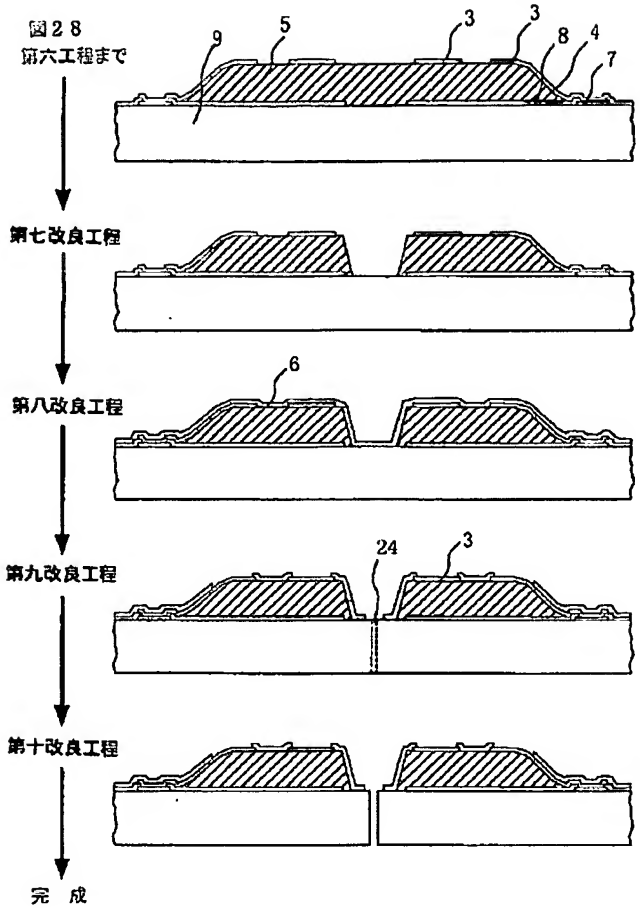
[Drawing 29]

図29



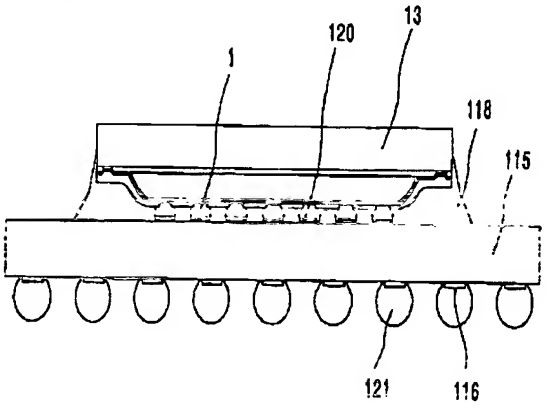
[Drawing 28]

図２８



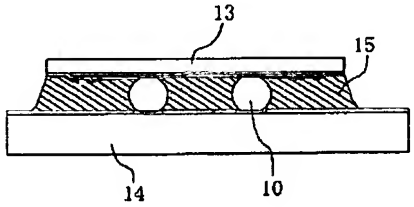
[Drawing 30]

図30



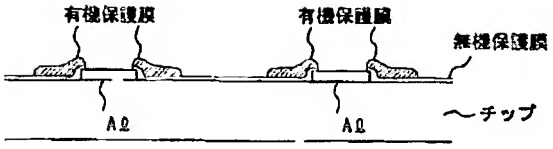
[Drawing 32]

図３２

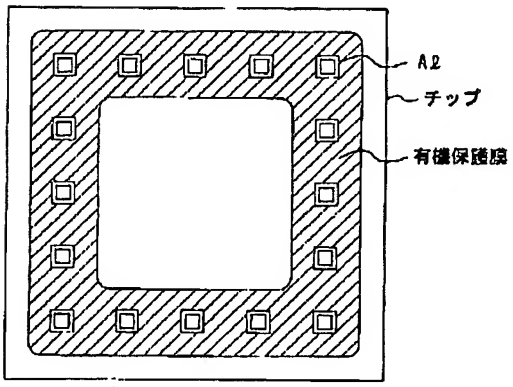


[Drawing 33]

図33

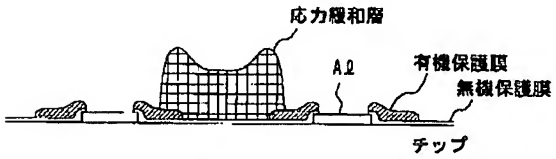


断面図



[Drawing 36]

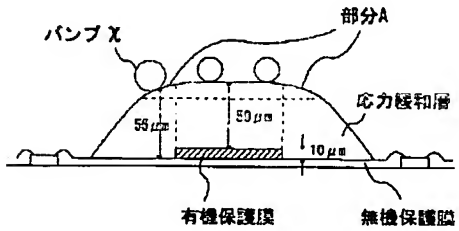
図36



断面

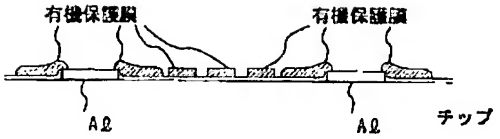
[Drawing 37]

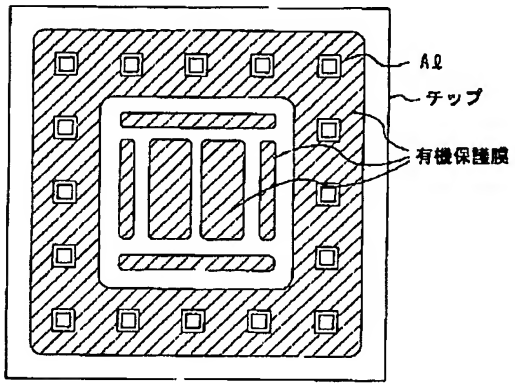
図37



[Drawing 34]

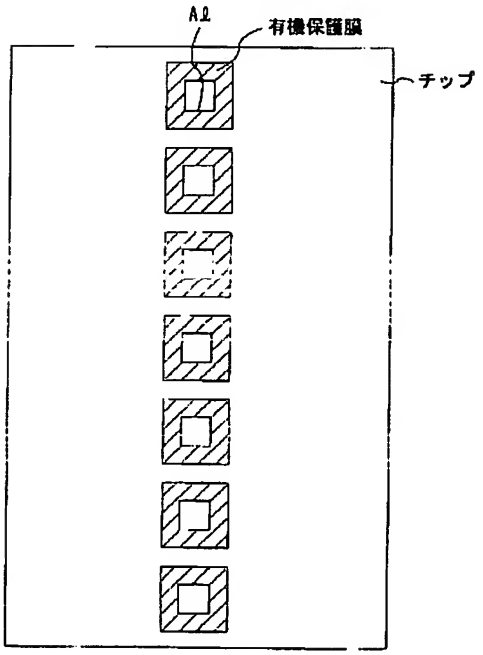
図34





[Drawing 35]

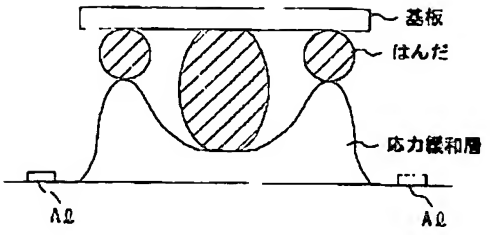
図35



上面図

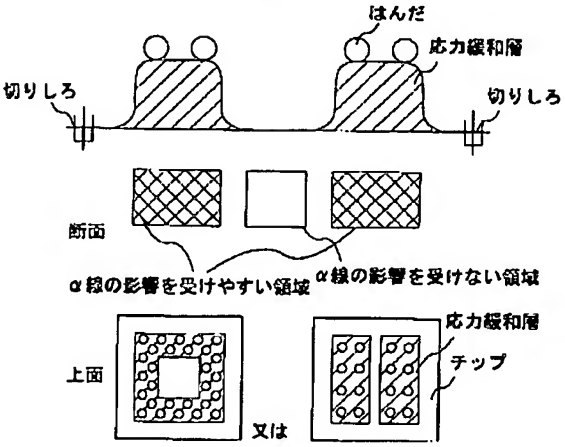
[Drawing 38]

図38



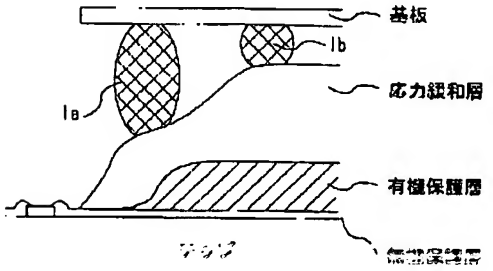
[Drawing 39]

図39



[Drawing 40]

図40



[Drawing 41]

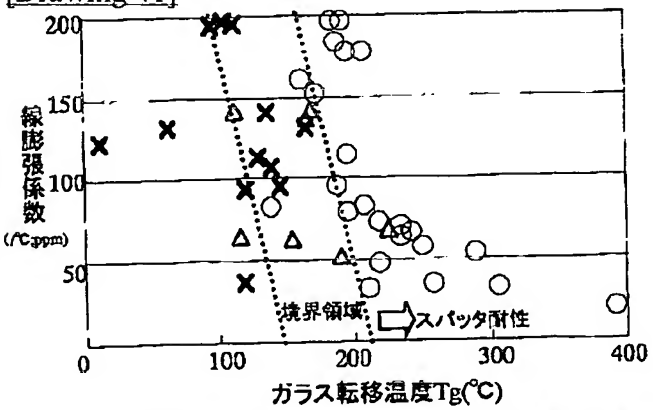


図41 応力緩和層候補材料の物性値とスパッタ耐性

(×;亀裂発生、△;膜発生、○;異常無)

[Translation done.]